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ULTRA WIDEBAND DIGITAL DELAY LINE

John B. Payne III

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Rome Air Development Center
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ULTRA WIDEBAND DIGITAL DELAY LINE

John B. Payne III

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FOREWORD

This report was prepared by Dr. John B. Payne, III, Techniques Branch, Rome Air Development Center, under Project 4506, Task 450601.

This report presents the detailed technical analysis, experimental results, and problems encountered in the design and construction of a four-bit digital delay line having an instantaneous, nondispersive, and lossless bandwidth of 400 mc/s. The frequency range covered was from 50 mc/s to 450 mc/s.

The author wishes to acknowledge the assistance of Michael Halayko, whose aid in obtaining experimental test data and reviewing the text of this report was invaluable.

This report has been reviewed and is approved.

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ABSTRACT

This report presents the detailed technical analysis, experimental results, and problems encountered in the design and construction of a four-bit digital delay line having an instantaneous, nondispersive, and lossless bandwidth of 400 mc/s. The frequency range covered was from 50 to 450 mc/s. The signal was switched either through or around the different time delay elements. The switches consisted of wideband amplifiers which minimize amplitude and phase fluctuations across the band and between the different signal paths. Switching was performed by purely electronic means with switching time less than 50 nanoseconds. Amplitude variations up to 400 mc/s were less than 1 db with a phase error of 2 degrees. At 450 mc/s the errors were 3 db and 10 degrees, respectively.

Also covered is the use of such a device for i-f time delay steering of wideband array antennas. Problems encountered in properly terminating wideband delay lines and component selection and layout are discussed.

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INTRODUCTION

In a previous report [1], RADC-TDR-64-218, Wideband, High Gain, Variable Time Delay Techniques for Array Antennas, June 1964, a technique for realizing a wideband, electronically variable digital time delay device was proposed.

Since the above report was published, an RADC study was made to determine the practicality of the techniques. This report presents the detailed technical analysis, experimental results, and problems encountered in the device as constructed and evaluated at RADC.

The device described herein had an instantaneous bandwidth of 400 mc/s and covered the frequency range from 50 to 450 mc/s. The Philco Corporation, under RADC sponsorship, is developing a similar digitally-variable device with a 400 mc/s bandwidth covering a 200 mc/s to 600 mc/s range.

INTRODUCTION

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BACKGROUND

The introduction of missiles and satellites into our defense environment has greatly increased the demand placed on modern radar technology. Longer detection ranges of smaller target cross sections and higher data rates have necessitated investigations into array antenna design. Array systems have the advantage of greater power handling capability and rapid single or multiple beam scanning from stationary structures.

Array antennas have been used for many years in both the communication and radar fields. Until recent years, this type of antenna was designed primarily to handle narrowband signals and, as such, was referred to as a phased array. The characteristics in this mode have been extensively studied and are well understood.

In adopting the array system, range resolution has suffered due to the bandwidth limiting problems encountered when narrow pulses or pulse compression like linear or quadratic frequency-time waveforms are incorporated into the phase steering system.

In an ideal array antenna, it is desirable to steer the position of the main beam by varying the time delay (i.e., where phase shifts greater than 360 degrees are obtainable), between elements. However, in narrowband systems, it has been shown that steering by varying the relative phase shift between elements (i.e., all phase shifts are less than 360 degrees) produces the same results with negligible loss in the signal-to-noise ratio. The relative phase shift method is simple and inexpensive to implement.

As the bandwidth of a phase steered array system is increased, a point is quickly reached where the loss in signal-to-noise can no longer be neglected. This deterioration in system performance of a phase steered array is caused by the finite propagation or transient time across the array aperture for off-boresighted beam positions. For a narrow pulse, it is this effect that produces a finite buildup and decay of the signal. For instance, when the pulse length is equal to the array transient time, the S/N will be down 3 db. For certain types of pulse compression, this finite transit time prevents coherent element-to-element summation off-boresight.

Another factor that is directly related to the transient time effect is the increase in half-power bandwidth (decreased antenna gain) due to an increase in the pulse bandwidth. In a phased steered array, the beam is phased to steer at a single carrier frequency. Power radiated at different frequencies in the spectrum will be steered to different directions. Thus, wider spectrum of transmitted frequencies results in beam broadening. Here, the frequency dependence is a function of beam position off-boresight and the type of steering employed.

These wideband problems can be overcome by the proper use of true time delay steering. However, the major component problem in building a wideband array system is the realization of a lossless, wideband, nondispersive, variable time delay device.

The purpose of this report is to discuss the design and experimental results obtained from a wideband digitally variable time delay device capable of steering array antennas.

The basic technique is shown in Figure 1. The input signal can be delayed through path 1 simply by closing S_1, S_2 and opening S_3, S_4. Path 2 is selected by closing S_3, S_4 and opening S_1, S_2. High-speed and wideband operation is obtained by using ultra wideband transistor amplifiers in place of the switches S_1, S_2, S_3, and S_4.

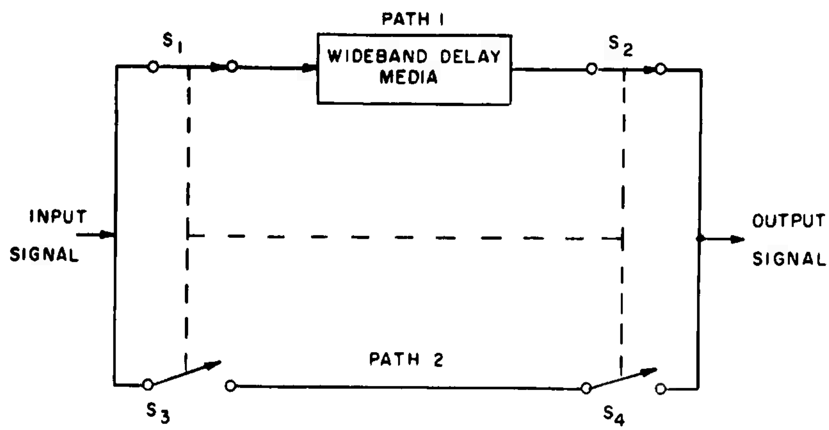

Figure 1. Single-Bit Digital Delay Line

The digital delay device described herein consisted of 2-binary bits, digitally controlled delays for use from 50 to 450 mc/s and having an instantaneous bandwidth of 400 mc/s. Only 2-binary bits were built since this investigation was aimed at proving feasibility. Larger bandwidths were not attempted for the same reason. This device provided four discrete time delay values in the range from 0 to 41 nanoseconds. The incremental delays could be changed easily by inserting different lengths of coaxial cable. Switching was performed by purely electronic means with switching times of 50 nanoseconds. The pertinent electrical characteristics of the digital delay line are:

Impedance level	50 ohms
Insertion gain	>0 db
Frequency range	50 to 450 mc/s
Instantaneous bandwidth	400 mc/s
Setup time	50 nsec maximum
Incremental delays	0, 12, 29, 41 nsec
Maximum phase error (deviation from linear)	2° up to 400 mc/s 10° at 450 mc/s
Amplitude variation across band	1 db to 400 mc/s 2 db at 450 mc/s

Amplitude error between bits	1 db to 400 mc/s 3 db at 450 mc/s
Power level	1 milliwatt
Power consumed	1 watt

Plots of amplitude and phase across the 400 mc/s bandwidth for each of the four delay settings are shown in Figure 27. Figures 28 and 29 show the digital delay line responses to a 65 mc/s and 400 mc/s bandwidth signal for each of the four delays.

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I. THEORETICAL ANALYSIS OF DIGITAL DELAY TECHNIQUE AND ASSOCIATED PROBLEMS

A. Variable Time Delay Requirements

To better understand the transient and propagation effects of wideband signals propagating across a phased array aperture and to calculate the required delay for off-boresight directions, consider Figure 2.

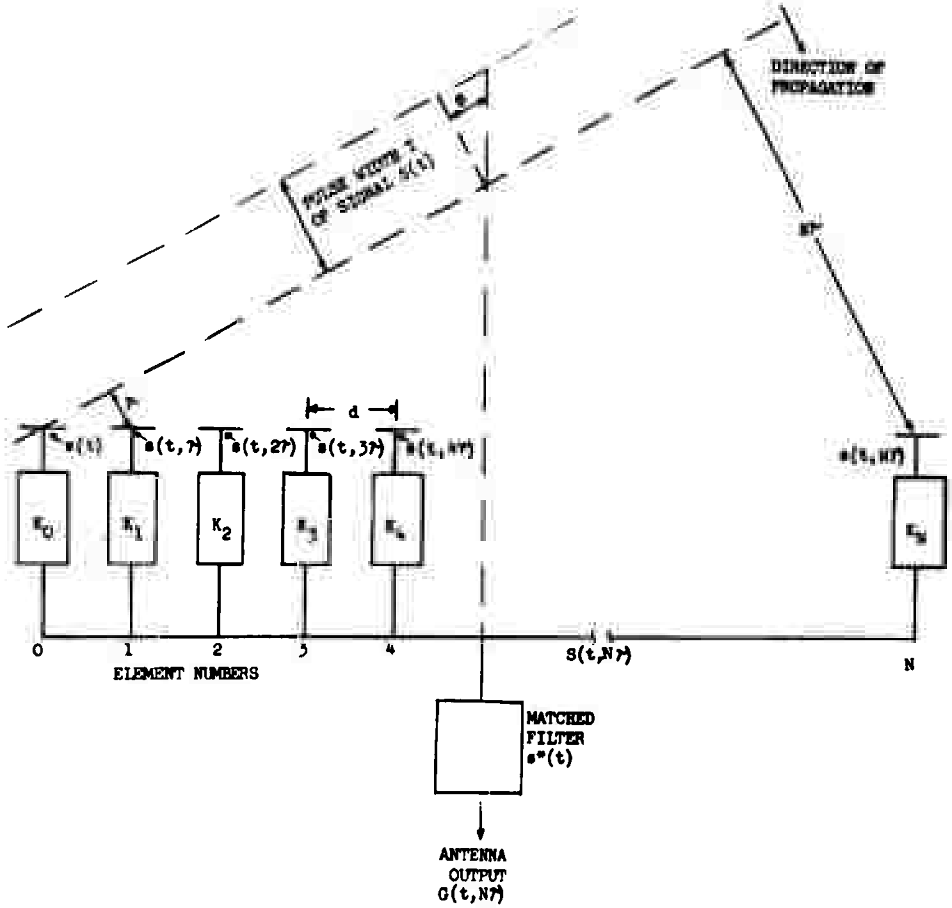

Figure 2. Array Antenna with Matched Filter After Element Summation

Here, an r-f pulse of width T, center frequency f_0, and bandwidth B (where B = 1/T) is impinging on the array interface phased to receive signals from an angle θ off-boresight. The array is considered to be steered by wideband phasing networks K_n that are lossless and introduce correct phase shifts of ϕ_n, at f_0 in each element. Here, n, denotes the element number. In a phase-steered array, redundant shifts, $n\phi$ greater than 360 degrees are eliminated so that $n\phi$ does not exceed 2π radians.

This is, in general, correct for most phased arrays since the phase shift is usually introduced before summing by shifting the LO signal of a mixer placed in each element. Ferrite shifters have this same characteristic.

In a phase-steered system for off-boresight beam positions, the leading edge of the signal wavefront will arrive at element 0 first as can be seen from Figure 2. The narrow pulse signal induced onto this element will be denoted by $g(t)$. At a time τ later, the signal will be induced onto element 2. This signal is given by $g(t + \tau)$. The arrival of the signal at the nth element is delayed by $n\tau$ and given by $g(t + n\tau)$. The element-to element signal delay τ is

$$\tau = \frac{d}{c} \sin\theta \qquad (1)$$

where, c, is the speed of light.

Each element signal is passed through the lossless phasing or time delay network K_n. If the network is a phase shifter, then only the r-f phase of each pulse is shifted; the signal delay is unaffected.

Upon combining each element signal in a linear summing network (the electrical length between each element and the summed output are considered equal), the resultant signal $G(t)$ is given by the expression

$$G(t, N\tau) = g(t) + g(t + \tau) + g(t + 2\tau) + \ldots g(t + N\tau). \qquad (2)$$

Due to the element-to-element delay for $\theta > 0$, this output will appear as a stepped ramp until steady state is reached in case of phase steering.

The summing networks output waveform for a six-element phase steered array will appear as shown in Figure 3. The energy contained in this output signal waveform is less than if the six pulses were in perfect time coincidence, as would be the case for $\theta = 0$. (Time coincidence for $\theta \neq 0$ can be obtained only by true time delays in each element.)* The further off-boresight the main beam is steered, the larger τ becomes and thus the more the waveform is smeared. This not only results in a decrease in signal energy but also reduces the range resolution properties. In other words, the array acts like a filter whose bandwidth decreases as θ increases.

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* For time delay steering, equation (2) can be written

$$G(t, N\tau) = g(t) + g(t + \tau - \tau_1) + g(t, 2\tau - \tau_2) + \ldots g(t + N\tau - \tau_N)$$

Coincidence at the summing networks output occurs when

$$\tau = \tau_1,\ 2\tau = \tau_2,\ \ldots\ N\tau = \tau_N$$

Thus,

$$G(t, N\tau) = Ng(t).$$

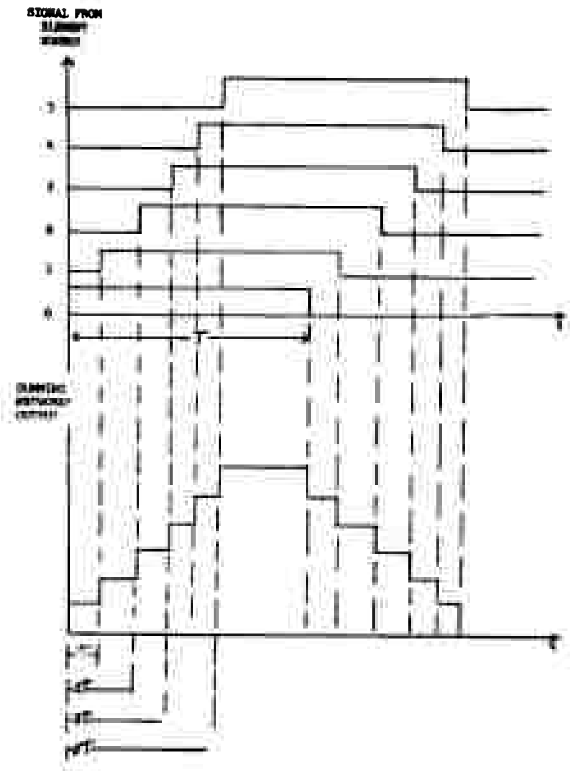

Figure 3. Propagation Effect of a Short Pulse on a Six-Element Array Antenna

The longer the CW pulse width (the narrower the bandwidth), the less effect the smearing or filtering and beam broadening have on the total energy content of the array output pulse. The longer pulse also increases the system's average power for a given PRF but decreases range resolution.

To calculate the delay required to steer the beam of an array antenna off-boresight by an angle, θ, a differential time delay, $n\tau$, must be introduced by the network, K_n, into each element or subgroup signal path. This delay is the sin θ of the propagation time across the antenna from the reference element, n=o, to the nth element. That is

$$n\tau = n\tau_o \sin\theta = \frac{nd}{c} \sin\theta \qquad (3)$$

where

c = speed of light in free space

τ_o = propagation time between elements or subgroups

d = element or subgroup spacing

If the reference element is moved to the center of the array and the beam steered about this reference as shown in Figure 4, the element delay must introduce both positive and negative delays, depending on the beam direction. If the nth element number, N, in a linear array is even (total number of elements being odd, i.e., $(N + 1)$, the center element position M_o is given by

$$M_o = \frac{N}{2}$$

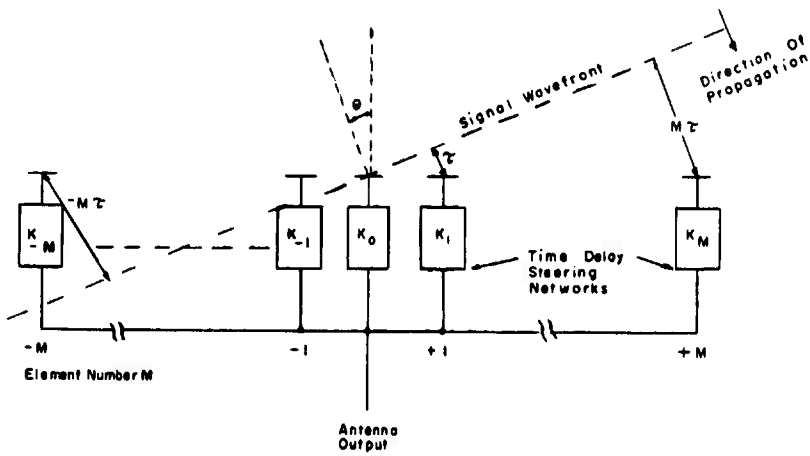

Figure 4. Array Antenna Diagram for Calculating Required Time Delay

The mth element of either side of M_o is given by

$$m \pm = \pm \left| n - \frac{N}{2} \right| .$$

The differential delay of the mth element or subgroup when steered about the center element becomes

$$m\tau = m\tau_o \sin\theta = \frac{md}{c} \sin\theta$$

Notice that the total differential delay required to scan $\pm\theta$ would be twice $m\tau$.

If we assume the array is $k\lambda$ long [i.e., $(N+1)d=(2M+1)d=k\lambda$] then for a scan angle of 45^o coverage, the maximum delay variation required can be written as

$$M\tau = \Delta T_{max} = 0.707\, k \frac{\lambda}{c} = 0.707 \frac{k}{f_o} . \tag{4}$$

Here the array is scanned about the center element.

This expression gives the maximum delay as a function of both the center frequency of operation and array length, k, in terms of wavelengths. Figure 5 is a plot of this equation for array lengths of 50, 100, 200, and 400 as a function of the operating frequency. Also indicated is the percent bandwidth where the signal is down 3 db due to the lack of time delay steering. This is indicated by δ.

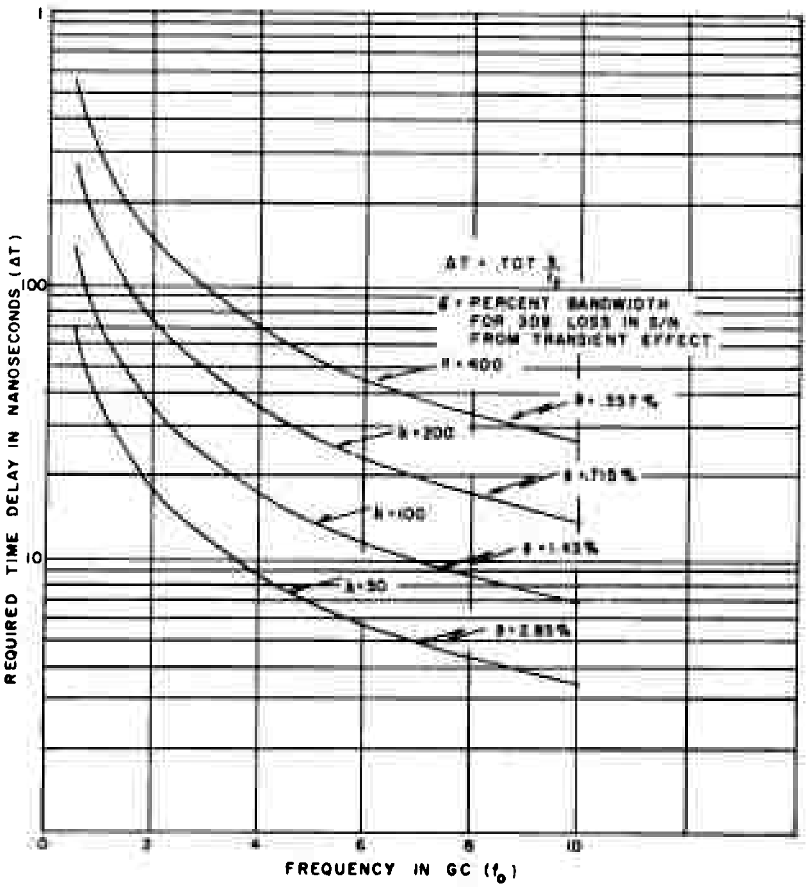

Figure 5. Plot for Array Lengths as a Function of Frequency

As an example, for 100 λ array at 4 GC (24.6 ft.) the maximum delay variation required is 17.65 nanoseconds. In the absence of delay steering, the signal would be down 3 db for bandwidth greater than 1.43% or 57 mc/s.

B. Wideband I-F Time Delay Steering

The digitally variable delay line being reported here is inherently a low frequency device. That is, it operates at the i-f frequency range of the array radar receiver. With bandwidths of 300 to 400 mc/s, the i-f frequency band normally would be in the 50 to 1000 mc/s range.

In this section, it will be shown that i-f time delay steering of an array antenna will pass a wideband signal and provide proper beam steering. It is found that an additional incremental phase shift must be introduced into the local oscillator of each mixer. In effect, the delay provides alignment of the envelopes while the local oscillator phase shifts provide coherence in phase summation. It is found that this condition is independent of bandwidth.

The block diagram of a wideband array receiving system using i-f time delay steering is shown in Figure 6.

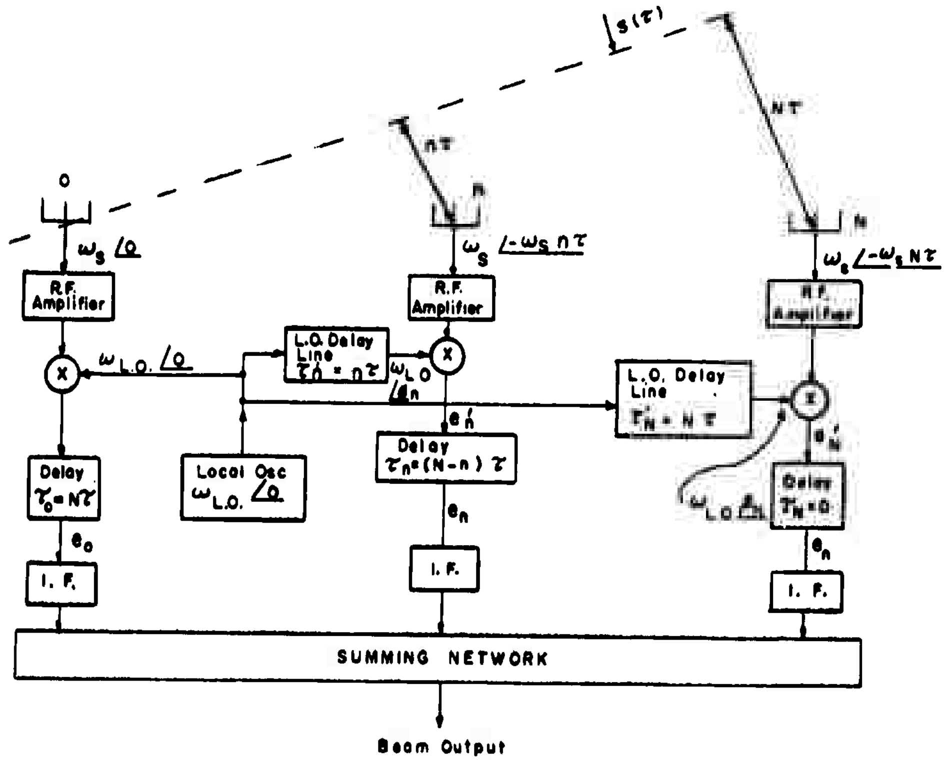

Figure 6. Wideband I-F Time Delay Beam Steering

For simplicity one delay line is shown in each element. In an actual system, the elements would probably be grouped in subarrays and each subarray then time delay steered. Each element in the array contains a low noise r-f preamplifier to establish the system noise figure and overcome mixer losses. The preamplifier is followed by a wideband mixer, a variable delay line with delay $\pm\tau_m$, and an i-f amplifier. The outputs of the delay lines are summed to produce a beam.

When the beam is steered off-boresight through the introduction of delays, $n\tau$, where

$$\Delta T_n = n\tau = \frac{nd}{c} \sin\theta, \qquad (5)$$

the delay line outputs will not in general add in phase even with the proper ΔT_n's to provide leading edge coincidence. An additional phase shift must be introduced by the local oscillator. This can be shown by considering the signal's phase relationship as it is processed.

We shall take the end element n = o of the array as reference. The impending waveform, as shown in Figure 6, reaches the nth element $n\tau$ seconds after it reaches the reference.

The delay lines are set to delay the signal in the n = o element path by $N\tau$. The delay line in the n = 1 line is set equal to $(N-1)\tau$. In the Nth line the delay is set equal to zero, and so on. In general, the Nth delay is set to $(N-n)\tau$. The result from each element is that the signals arrive at the summing network simultaneously.

With the proper delays set in each signal path to align the signal envelopes, the reference element delay line output is

$$e_o = (\sin \omega_s t \sin \omega_{LO} t)\, U_{IF}\,(t - N\tau) e^{-j\omega_{IF} N\tau} = U_{IF}\,(t - N\tau) \cos \omega_{IF}\,(t - N\tau). \tag{6}$$

Here ω_s is the signal frequency, ω_{LO} the local oscillator frequency. The sum frequency has been filtered out. Both of these signals are taken as the reference and have zero phase shift.

If all of the local oscillator signals are in phase with the reference local oscillator, ω_{LO}, the signal at the input to the nth delay line is

$$e'_n = U_s\,[t - n\tau]\, e^{-j\omega_s n\tau} \sin \omega_s t \sin \omega_{LO} t = U_s\,[t - n\tau] \cos [\omega_{IF} t - \omega_s n\tau]. \tag{7}$$

When passed through a delay of (N-n)T seconds in order to align the envelopes, the signal at the delay lines output becomes

$$en = \underbrace{U_s\,[t - n\tau]\, e^{-j\omega_s n\tau} \sin \omega_s t}_{\text{signal}}\, \underbrace{\sin \omega_{LO} t}_{\text{L. O.}}\, \underbrace{U_{IF}\,[t - (N - n\tau)]\, e}_{\text{Delay line}}{}^{-j\omega_{IF}(N-n)\tau} \tag{8}$$

$$= U_{IF}\,(t - N\tau) \cos [\omega_{IF}\,(t - N\tau) - \omega_{LO}\, n\tau].$$

Comparing equations (6) and (8), it can be seen that the phase between the reference element and the nth element differ by $\omega_{LO}\, n\tau$. For coherent addition of these two signals, this phase difference must be reduced to zero. It is important to note that for a fixed local oscillator signal frequency, the phase difference between these two signal paths is independent of the r-f carrier or i-f frequency. In other words, such a system (if $\omega_{LO}\, n\tau = 0$) is not bandwidth-limited.

If an arbitrary phase shift, ϕ_n, is introduced between the reference local oscillator signal ($\omega_{LO} \underline{|0}$) and the local oscillator of the nth element ($\omega_{LO}\big|_n = \omega_{LO} \underline{|\phi_n}$), the signal at the delay line output, n, is given by

$$e_n = \underbrace{U_s\,[t - n\tau]\,e^{-j\omega_s n\tau} \sin\omega_s t}_{\text{signal}}\ \underbrace{\sin(\omega_{LO} t + \phi_n)}_{\text{L.O.}}\ \underbrace{U_{IF}\,[t\,(N-n)\tau]\,e}_{\text{Delay line}}{}^{-j\omega_{IF}(N-n)\tau} \tag{9}$$

$$= U_{IF}\,(t - N\tau)\cos\,[\omega_{IF}\,(t - N\tau) = \omega_{LO} n\tau + \phi_n]\,.$$

To obtain coherent summation between the reference and nth element, the phase term of equation (9) must reduce to zero. That is,

$$\phi_n - \omega_{LO} n\tau = 0$$

or

$$\phi_n = \omega_{LO} n\tau. \tag{10}$$

In other words, to produce element-to-element summation, the phase of the local oscillator signal must be shifted by $\omega_{LO} n\tau$.

If the reference local oscillator were passed through a narrowband adjustable delay line τ'_n to obtain the desired phase shift

$$\tau'_n = \frac{d\phi_n}{d\omega_{LO}} = n\tau. \tag{11}$$

As can be seen for an array where the reference or zero delay element is located at the center, the delay required to shift the local oscillator of the nth element is just that inserted in the signal path of the (N - n) element. The local oscillator delay or equivalent phase shift network can be a narrowband device. Since all phase shifts are cancelled out by this method, the <u>relative</u> signal phases are independent of frequency. Therefore, this technique is applicable for processing wideband signals.

The introduction of the delay lines in the local oscillator paths would result in the transmission of a beam steered to the θ direction if the mixer local oscillator signal were radiated by its antenna element

The variation of relative phase or phase error between the reference and nth element is given as the phase terms in equation (9).

$$\phi_{error} = \underbrace{\omega_s n\tau}_{\text{signal}} - \underbrace{\phi_n}_{\text{L.O.}} + \underbrace{\tau_n}_{\text{I.F.}} = \underbrace{\omega_s n\tau}_{\text{signal}} - \underbrace{\omega_{LO} n\tau}_{\text{L.O.}} + \underbrace{\omega_{IF}\,(N-n)\tau}_{\text{IF Delay}}\ . \tag{12}$$

It is important to note that a degree of phase shift at the r-f or local oscillator frequency produces a degree of phase shift at i-f, also, the delay line at i-f must have the same phase stability as if the delay were done at r-f. Phase stability is easier to obtain and maintain at the lower i-f frequency than at the higher r-f frequency.

Since the transmit process is the reciprocal of the receive case, the above analysis holds for both. In the transmit case, a degree error in $\omega_{IF}(N-n)\tau$ will result in only a degree phase error at r-f, $\omega_s n\tau$.

Regarding the local oscillator phase shift, since the LO signal is a CW signal, the redundant 2π radian shifts can be eliminated by using only a 2π modulus shifter in the line. However, if a delay line is used in the nth element LO, that is, identical to the signal delay line used in the (N - n) element, the programming is much easier since the two require the same setting of a given θ. The successive LO phase shifts can also be obtained by series feed shifts.

C. Wideband Digitally Controlled Delay Line Approach

Digitally controlled delay lines or phase shifters have been used for the past several years in steering phased array antennas. Lincoln Laboratory has conducted an extensive program in the development of such devices. Much of Lincoln's work can be found in their technical reports.

Most digital delay line or phase shift devices use diodes to switch the signal through or around a length of transmission line cut to give the desired incremental delay or phase shift. A commonly used technique is shown in Figure 1. The input signal can be delayed through path 1 simply by closing S_1, S_2. Path 2 is selected by closing S_3, S_4, and opening S_1, S_2. However, high-speed switching requires the elimination of mechanical switching devices. Switching devices in the past have utilized simple diodes with small forward impedance and a high back impedance. Replacing S_1, S_2, S_3, S_4, with diodes D_1, D_2, D_3, D_4, and controlling the magnitude and direction of current flow through the diodes enables directing the input signal through either path 1 or path 2.

These diodes, however, have a finite series resistance when forward biased and, therefore, produce loss. Additional loss is usually introduced so as to reduce the fluctuation in amplitude as the signal path is changed.

The matching of these diodes and the proper termination of the incremental delay units is accomplished at the expense of bandwidth. Series diode resistance plus diode and stray reactance also result in poor matching and SWR between the incremental delay units. A finite SWR will produce ripples in amplitude as well as phase linearity across the band.

A typical 6-bit, 28 mc/s digital phase shifter or delay line is described in Lincoln Laboratory Technical Report 228. It was designed to produce a total of 360° phase shift at 28 mc/s by switching either through or around six lengths of coax by the use of diode switches. Total insertion loss was 11 db. The set-up time ran about 3 μsec with a maximum amplitude error of 0.25 db and phase error of 2°. Input power capacity was limited to one watt. Each diode switch required about 40 ma in order to reduce the diode series resistance to a usable value.

The wideband digital delay line to be described utilizes the basic technique indicated by Figure 1. However, in this case, each mechanical switch is replaced by a wideband amplifier. It is the bandwidth of these amplifiers that determines the system bandwidth. These amplifiers can be gated on or off. By using wideband amplifiers in place of the diode switches, three advantages are gained: (1) Each delay

line (coax) is properly terminated into its characteristic impedance over the frequency band of interest; this prevents loss due to excessive SWR; (2) Each delay line increment is isolated from the next due to the presence of amplifiers; (3) With the inclusion of amplifiers, the total input-output gain can be made equal to or greater than unity (gains as high as 100 db for a 10-bit device are achievable with bandwidths of hundreds of megacycles; however, 100 db is more than is normally required with such bandwidths).

The wideband digital delay line is inherently a low-frequency device. By low frequency we mean i-f frequencies up to 400 or 800 mc. If we wish to process a signal with a 200 or 300 mc bandwidth, the i-f center frequency would more than likely be located in the range of 200 to 300 mc.

It can be seen that if the digital delay line device produces sufficient gain, then an additional wideband i-f amplifier is no longer required. This would reduce the cost per element.

The angular beam coverage generally required is $\pm 45^{\circ}$ or a total of 90°. If the array is 100λ, then the 3-db beam width would be about 0.5°. If the beam were moved in 0.1° increments, the resultant scanning would closely resemble a continuous scanning system. This would require 900 beam positions. If each digital delay line had 10 bits, this would give 1,024 discrete positions. Nine bits would give 512 positions or about 0.2° incremental beam steps.

D. Wideband Delay Elements

Previously, the wideband delay line for insertion between amplifiers Q_1 and Q_2 has not been considered. Any delay device considered should not be too lossy; however, this is of secondary importance with the addition of amplifiers. Of primary importance is the dispersion of these devices. They should be operated well in the nondispersive region. The most obvious method for realizing a wideband delay line would be the use of a fixed length of coax cable. Different lengths of cable would produce different delay times.

Over a wide frequency range, the attenuation of coaxial cable is a function of frequency. For instance, RG-9/U which has a characteristic impedance of 52 ohms and 29.5 pfd/ft. has an attenuation per 100 ft. of 0.16 db at 1 mc; 0.55 db at 10 mc; 2 db at 100 mc; and 8.6 db at 1 GC. A second consideration would include the size of the cable, since a 50-foot coil could take up quite a bit of room. Some manufacturers produce small low-capacitance cable.

A coaxial cable with a high dielectric constant is desirable since this will reduce the propagation velocity and thus result in shorter lengths of cable. RG-8/U has a relative propagation velocity of 65.9%.

By mismatching wideband transformers, they can be made to give a slight increase in gain with frequency. This effect could be used to compensate the attenuation characteristics of the cable to a limited degree.

Generally, helical high-impedance delay cables (center conductor wound like a helix) are dispersive above a critical frequency. The upper critical frequency is seldom over 10 mc which would eliminate it from consideration. However, variations of this technique could no doubt be devised to extend the frequency to several hundred megacycles.

Strip-line transmission lines have the advantage of compact size and easily variable characteristic impedance. Their bandwidth can also be made quite large.

The Philco Corporation, under RADC sponsorship, has been developing an electronically variable time delay technique using an all-pass network similar to the symmetrical lattice phase correction network. Philco has published a description of their device [6].

A similar delay technique has been described by R. W. Calfee [7]. The lumped-parameter delay line technique appears attractive as a delay device. A typical network is capable of producing delays from 8 to 15 nanoseconds, or a variation of 7 nanoseconds, with a bandwidth of 30 to 40 mc. The variation in delay is produced by replacing the fixed capacitors with matched varactors. To extend the bandwidth to several hundred megacycles requires high-quality diodes that become quite expensive. As the frequency is increased, the delay is decreased approximately proportionally. If the expensive varactors were replaced by small adjustable capacitors, the total delay through the device could be used to obtain a desired incremental delay. With adjustable capacitors, each increment of delay could easily be adjusted to the proper value.

The coaxial cable technique could be combined with the adjustable lumped constant network. This would reduce the complexity of final adjustment by providing a simple method of line stretching.

E. Effects of Improper Delay Line Termination

Before we can consider the amplifier configuration used to replace the switches shown in Figure 1, the SWR problem present in the delay lines must be considered. Although the discussion below is in terms of a coaxial transmission line, it is applicable to any delay median.

In general, most driving sources are impedance sensitive and their output varies with output impedance.

When large percent bandwidth (100 percent or greater) signals are passed through a transmission line, it is of little consequence that the SWR be held constant across the band if it is anything greater than unity. This can be seen by considering the expression for the normalized impedance at the input to a lossless transmission line of length 1, frequency ω and termination Z_r [2].

$$\frac{Z_{in}}{Z_o} = \frac{\dfrac{Z_r}{Z_o} + j \tan \dfrac{\omega \ell}{C}}{1 + j \dfrac{Z_r}{Z_o} \tan \dfrac{\omega \ell}{L}} = \frac{\dfrac{Z_r}{Z_o} + j \tan \dfrac{2\pi \ell}{\lambda}}{1 + j \dfrac{Z_r}{Z_o} \tan \dfrac{2\pi \ell}{\lambda}} \quad . \tag{13}$$

A perfect termination is seldom possible. This is particularly true when the line is terminated into a lumped resistor or non-precision termination. In the above expression Z_{in} is seen to be constant if $Z_r = Z_o$ and independent of frequency. However, when $Z_r \neq Z_o$, the line input impedance varies with frequency and line length. Note that if the termination is partly reactive, i.e., L or C, then Z_r is a function of frequency ($Z_r = j\omega L$ or $1/j\omega C$) and Z_{in} becomes an increasing oscillatory function of frequency.

A plot of equation (13) in polar form is known as a Smith Chart (Figure 7). By use of the Smith Chart, one can easily determine the input impedance and phase angle variation with frequency as the load impedance is changed.

As an example, let us assume our terminating impedance to be purely resistive over the frequency band of interest producing, for example, a VSWR of 1.3. That is,

$$\sigma = 1.3 = \frac{Z_r}{Z_o} = \frac{V_{max}}{V_{min}} \tag{14}$$

for a purely resistive load. Figure 7 shows the circle for $|\sigma| = 1.3$ drawn. The magnitude and phase angle of the line impedance for a given line length and frequency can be measured. The outer radius of the circle reads line length in terms of wavelength; that is ℓ/λ.

IMPEDANCE OR ADMITTANCE COORDINATES

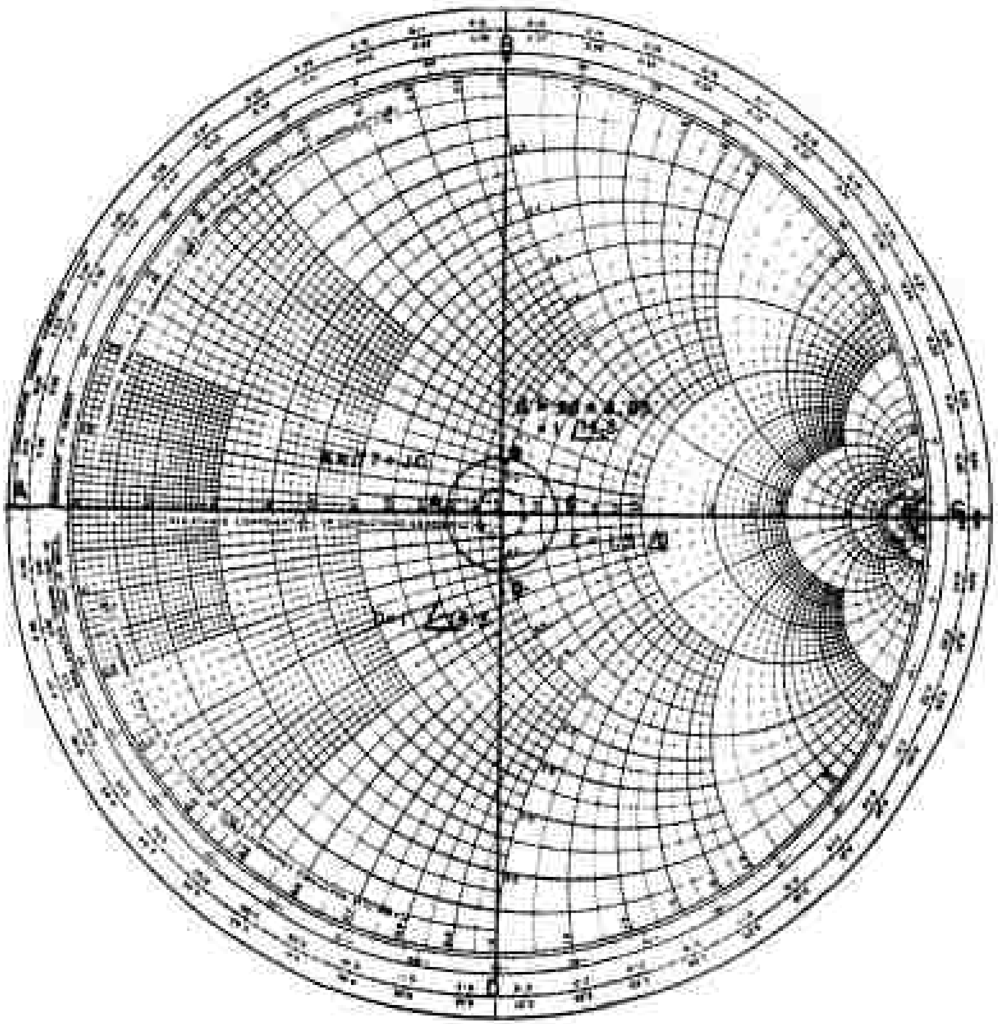

Figure 7. Smith Chart

Strip-line transmission lines have the advantage of compact size and easily variable characteristic impedance. Their bandwidth can also be made quite large.

The Philco Corporation, under RADC sponsorship, has been developing an electronically variable time delay technique using an all-pass network similar to the symmetrical lattice phase correction network. Philco has published a description of their device [6].

A similar delay technique has been described by R. W. Calfee [7]. The lumped-parameter delay line technique appears attractive as a delay device. A typical network is capable of producing delays from 8 to 15 nanoseconds, or a variation of 7 nanoseconds, with a bandwidth of 30 to 40 mc. The variation in delay is produced by replacing the fixed capacitors with matched varactors. To extend the bandwidth to several hundred megacycles requires high-quality diodes that become quite expensive. As the frequency is increased, the delay is decreased approximately proportionally. If the expensive varactors were replaced by small adjustable capacitors, the total delay through the device could be used to obtain a desired incremental delay. With adjustable capacitors, each increment of delay could easily be adjusted to the proper value.

The coaxial cable technique could be combined with the adjustable lumped constant network. This would reduce the complexity of final adjustment by providing a simple method of line stretching.

E. Effects of Improper Delay Line Termination

Before we can consider the amplifier configuration used to replace the switches shown in Figure 1, the SWR problem present in the delay lines must be considered. Although the discussion below is in terms of a coaxial transmission line, it is applicable to any delay median.

In general, most driving sources are impedance sensitive and their output varies with output impedance.

When large percent bandwidth (100 percent or greater) signals are passed through a transmission line, it is of little consequence that the SWR be held constant across the band if it is anything greater than unity. This can be seen by considering the expression for the normalized impedance at the input to a lossless transmission line of length 1, frequency ω and termination Z_r [2].

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A perfect termination is seldom possible. This is particularly true when the line is terminated into a lumped resistor or non-precision termination. In the above expression Z_{in} is seen to be constant if $Z_r = Z_o$ and independent of frequency. However, when $Z_r \neq Z_o$, the line input impedance varies with frequency and line length. Note that if the termination is partly reactive, i.e., L or C, then Z_r is a function of frequency ($Z_r = j\omega L$ or $1/j\omega C$) and Z_{in} becomes an increasing oscillatory function of frequency.

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$$\sigma = 1.3 = \frac{Z_r}{Z_o} = \frac{V_{max}}{V_{min}} \tag{14}$$

for a purely resistive load. Figure 7 shows the circle for $|\sigma| = 1.3$ drawn. The magnitude and phase angle of the line impedance for a given line length and frequency can be measured. The outer radius of the circle reads line length in terms of wavelength; that is ℓ/λ.

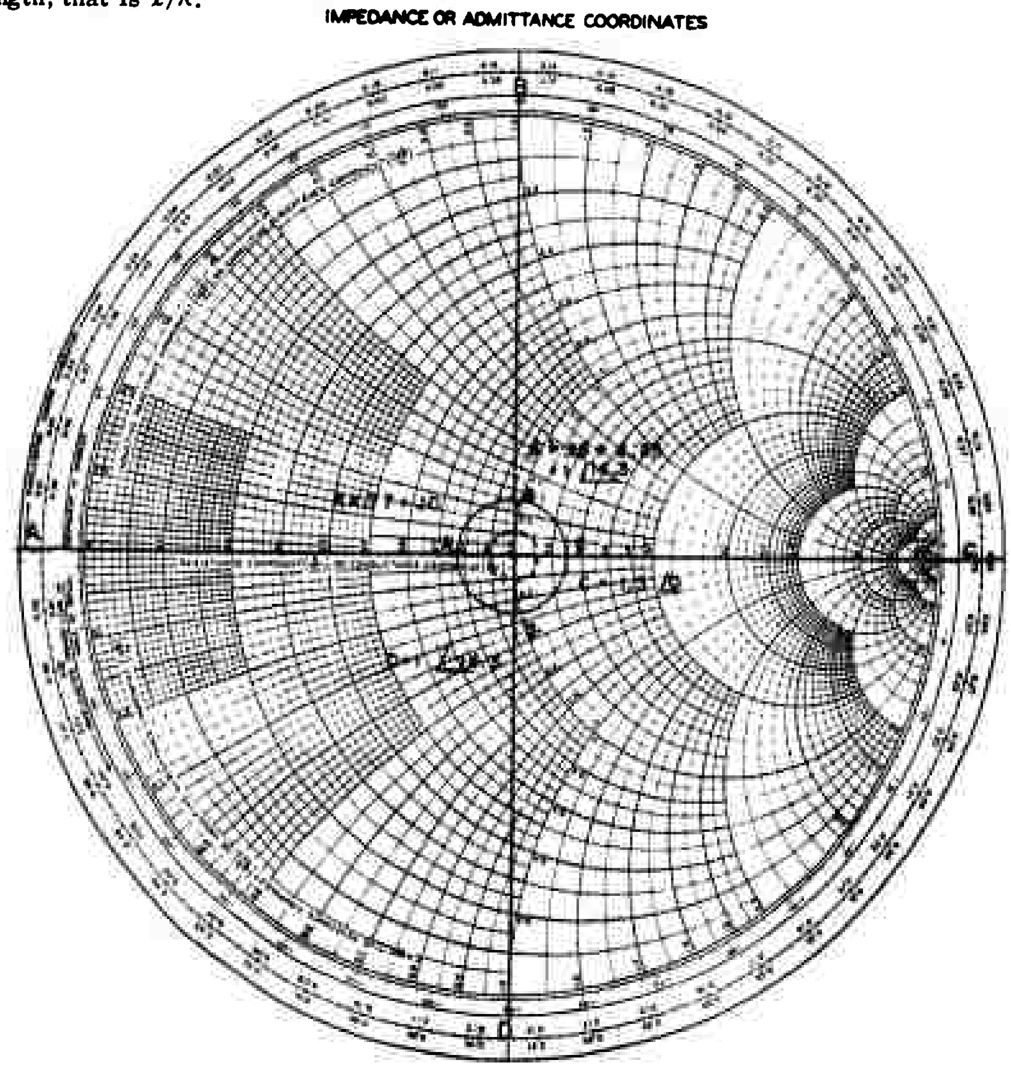

Figure 7. Smith Chart

Since, in most applications, the line length is held constant, let us assume as an example that

$$\ell = 2\lambda_o \tag{15}$$

at f_o. Figure 8 shows how the magnitude and phase angle of the input impedance, $|Z_{in}|/Z_o$ varies with frequency over a 100 percent bandwidth.

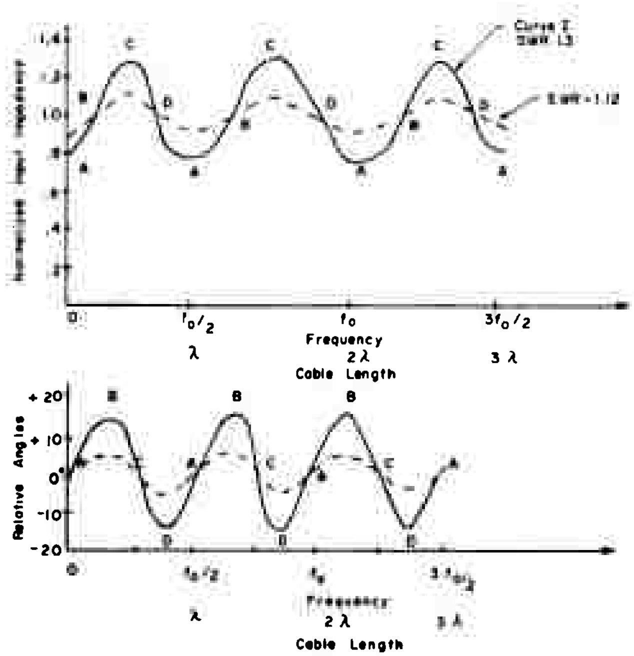

Figure 8. Input Impedance Variation of a Transmission Line of Length $\ell = 2\lambda_o$ for $Z_r = 1.3Z_o$

The frequency axis has been relabeled to indicate cable length in terms of wavelength. Impedance is then read from the Smith Chart by first drawing a circle of constant SWR equal to 1.3 about the center of the chart. A line is then drawn from the center to a point on the chart radius corresponding to the desired wave-length. The impedence Z_{in} at the input to the transmission line is indicated by the intersection of this line and circle.

For a purely resistive load, the ratio of maximum voltage to minimum voltage due to a variation with frequency is just the VSWR, σ.

$$\sigma = \frac{Z_r}{Z_o} = \frac{V_{max.}}{V_{min.}} \tag{16}$$

The ratio of maximum input impedance to minimum input impedance is given by

$$\frac{Z_{in}\big|_{max}}{Z_{in}\big|_{min}} = \frac{V_{max}}{I_{min}} \cdot \frac{I_{max}}{V_{in}} = \sigma^2 = \left(\frac{Z_r}{Z_o}\right)^2 . \tag{17}$$

If the line is driven from a constant voltage source, the output voltage variation will be given by the VSWR, σ. This can be seen since the input voltage is given by the sum of the incident and reflected waves V_1 and V_2. When driven from a constant voltage source, the sum remains constant, i.e.,

$$V_1 + V_2 = K$$

Since

$$V_2 = \rho V_1$$

where ρ is the ratio of reflected voltage to incident voltage due to mismatch. Therefore,

$$V_1 \ (1 \pm \rho) = K.$$

The voltage across the termination Z_r is

$$V_1 \ (1 - \rho) = V_r$$

and seen to be dependent on V_1 which varies from

$$V_1\big|_{min} = \frac{K}{(1 + \rho)}$$

to

$$V_1\big|_{max} = \frac{K}{(1 - \rho)}$$

Therefore, the output voltage variation is

$$\frac{V_{max}}{V_{min}} = \frac{1 + \rho}{1 - \rho} = \sigma$$

for a purely resistive load.

If the driving source is the current generator, the same result is obtained.

If the driving source voltage gain is proportional to the load impedance, then the output voltage across the line termination will remain constant.

It has been found that the power gain of most wideband transistor amplifiers varies with load impedance. For this reason, we shall briefly investigate the input impedance variation of a transmission line with frequency. We shall write

$$\frac{Z_{in}\big|_{max}}{Z_{in}\big|_{min}} \text{ in db} = 20\ell n\,\sigma = 10\ell n\,\frac{Z_{in}\big|_{max}}{Z_{in}\big|_{min}}\ . \tag{18}$$

Therefore, a termination of $1.12\ Z_r = Z_o$ produces an impedance variation of 1 db across the band. Equation (18) is plotted in Figure 9.

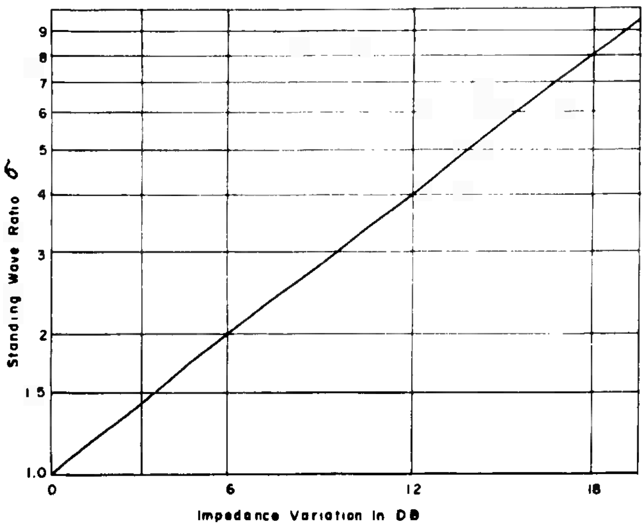

Figure 9. Standing Wave Ratio σ in db

So far we have discussed the case where the terminating impedance consisted of a purely resistance load. Let us now consider how the input impedance varies with frequency when a reactive component is shunted across or in series with the resistive load as shown in Figure 10. This is the condition encountered at the input to a transistor amplifier.

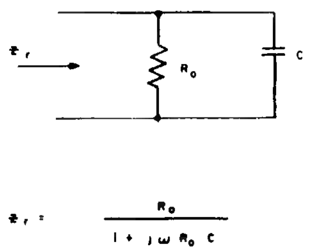

Figure 10. Complex Transmission Line Load

Here, the load is seen to be a function of frequency. For frequencies well below $\omega_C = 1/R_oC$

$$Z_r = R_o.$$

The line will thus be perfectly terminated until ω approaches ω_c at which point the VSWR will increase.

As an example, let us consider the input impedance of a line that is 2λ long at f_0. Also consider C to be of such a value that

$$\omega_0 = 0.1\,\omega_c = \frac{0.1}{R_0 C}$$

$$Z_r = \frac{R_0}{1 + J.1\,\frac{\omega}{\omega_0}} \quad . \tag{19}$$

For use on the Smith chart

$$Y_R = \frac{R_0}{Z_r} = 1 + J.1\,\frac{\omega}{\omega_0} \quad . \tag{20}$$

A plot of the line input impedance with frequency as given by equation (13) with the complex load of equation (20) is shown in Figure 11 below:

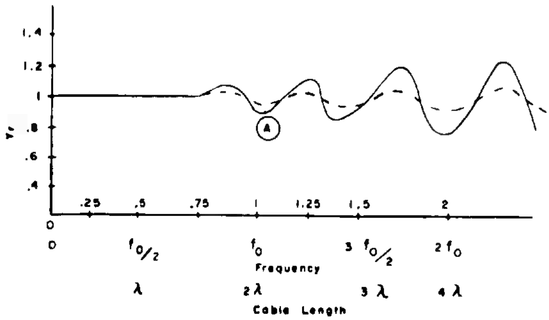

Figure 11. VSWR on Transmission Line as a Function of Frequency Due to a Complex Load

For this example, where $\omega_c = 0.1\,\omega_0$, the admittance variation in the region of the band edge ($3\,f_0/2$) is about 3.0 db and is increasing with frequency.

A simple technique for reducing the line impedance variation problem is to introduce a matched attenuation into the line as shown in Figure 12.

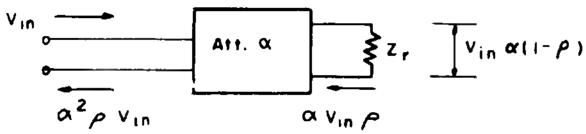

Figure 12. Technique for Reducing Impedance Variation

The reflected wave experiences additional attenuation and has a magnitude $\alpha^2 \rho V_{in}$, where ρ is the reflection coefficient at the load Z_r. The VSWR thus becomes

$$\sigma_{att} = \frac{1 + \rho\alpha^2}{1 - \rho\alpha^2} \ . \tag{21}$$

Since

$$\rho = \frac{Z_r/Z_o - 1}{Z_r/Z_o + 1} \tag{22}$$

$$\sigma_{att} = \frac{Z_r/Z_o\ (1 + \alpha^2) + (1 - \alpha^2)}{Z_r/Z_o\ (1 - \alpha^2) + (1 + \alpha^2)} \ . \tag{23}$$

Since for purely resistive loads

$$\sigma = Z_r/Z_o$$

$$\sigma_{att} = \frac{\sigma\,(1 + \alpha^2) + (1 - \alpha^2)}{\sigma\,(1 - \alpha^2) + (1 + \alpha^2)} \ . \tag{24}$$

Note that as the attenuation increases, i.e., α decreases, the resultant standing wave ratio approaches one as would be expected.

If a given standing wave ratio, σ, is present without the attenuation, the ripple may be reduced to the desired level, σ_{att}, by the insertion of attenuation α. Solving equation (24) for α yields

$$\alpha^2 = \frac{(\sigma_{att} - 1)\ (\sigma + 1)}{(\sigma_{att} + 1)\ (\sigma - 1)} \cdot \quad \sigma_{att} < \sigma \qquad . \tag{25}$$

This expression is plotted in Figure 13 for $\sigma_{att} = 1$ db. That is, for a given σ, the resultant α must be inserted in the line to reduce the VSWR to 1 db.

In order to reduce the impedance variation shown in Figure 8 to 1 db, a 4.6 db of attenuation must be inserted in the line as indicated in Figure 13. The dotted curve of Figure 8 shows the resultant impedance variation with frequency. Likewise, the dotted curve of Figure 11 indicates how the impedance variation is reduced for a complex load. Although not indicated, the phase variation will also be reduced. With a complex load, the introduction of attenuation will cause the peaks and nulls to shift.

If the attenuator were replaced by a broadband isolator or circulator at the input to the line, the reflected wave would be attenuated and a negligible impedance variation would result.

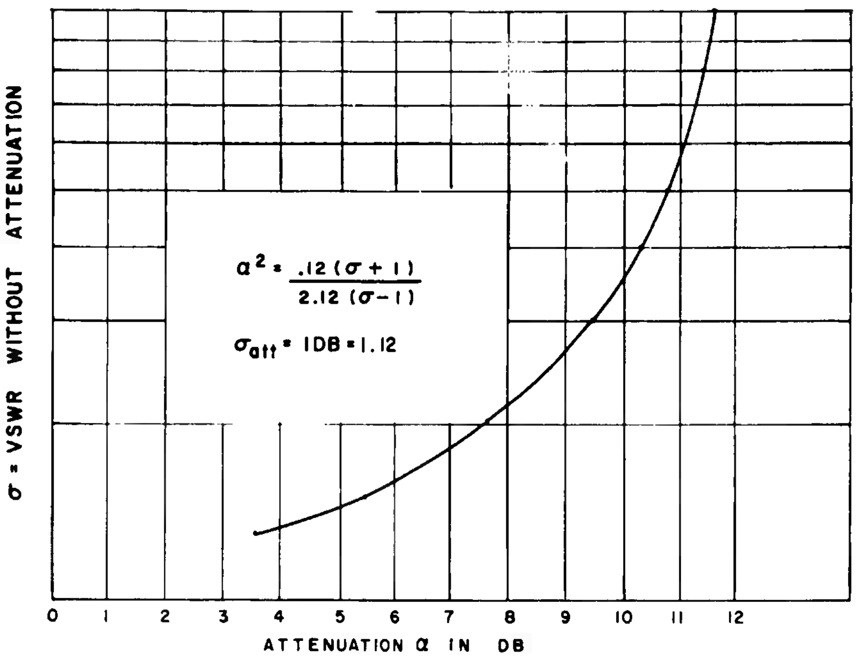

Figure 13. Attenuation Required to Reduce σ_{att} to 1 db

It has been found in practice that if the attenuator is located at the load, and α is much greater than 10 db, connector discontinuities become the dominant factor. As far as line impedance variation is concerned, it is immaterial whether the attenuation is located at the load or input end of the transmission line. In practice, it is best to locate the attenuator at the input end to minimize connector effects.

A simple technique for measuring the impedance variation of a line with frequency is shown in Figure 14.

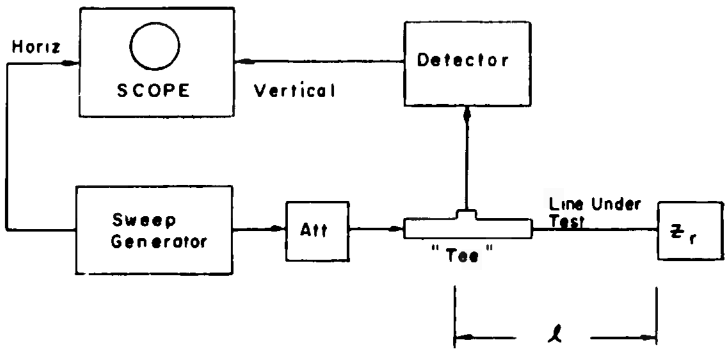

Figure 14. Technique for Measuring Impedance Variation

The test cable and termination are driven from a sweep generator which sweeps the desired frequency range. Since the output of a sweep generator usually has a constant output voltage, an attenuator is placed at its output to allow a voltage variation at the "Tee" connector. A detector measures the input voltage to the cable which is approximately equal to the sum of the incident and reflected wave. The detector output variation is thus a function of the input impedance variation as given by equation (14).

F. Configuration of One-Bit Digital Delay System

When wideband amplifiers are used to replace the mechanical switches of Figure 1 and the results of the preceding section are considered, a single bit of the digital delay system takes the form shown in Figure 15.

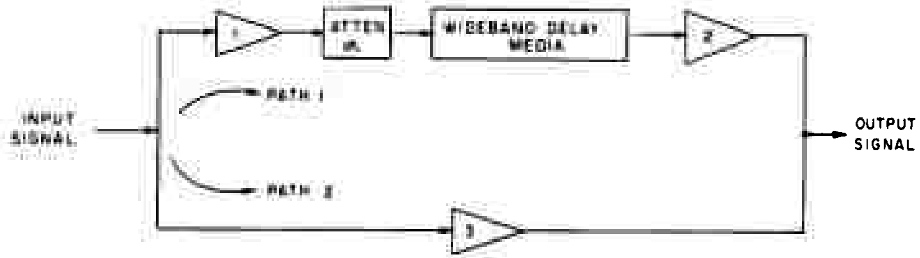

Figure 15. Single-Bit Digital Delay Line

It can be seen that the attenuator, α has been placed at the input to the delay media to reduce the magnitude of the reflected wave. In the lower signal path, one amplifier has replaced both switches.

The selection and design of an overall digital delay line could assume many configurations. Each bit or group of bits could be designed as an integral unit with specified input and output impedances whereby any desired number of units could be cascaded. On the other hand, the complete system could be designed as an integral unit.

Apparently the most practical approach for such a system would be to design either each bit or several bits as a unit. By cascading basic units, such a system would be more flexible.

In the digital delay system described here, a two-bit digital unit was designed, constructed, and tested. Because of lack of time, only one such unit was built and tested. With proper output and input impedances, many such units could be cascaded to yield the desired number of bits.

When designing each bit of such a system, it is important to make the resultant signal polarity of each signal path the same. That is, if both amplifiers 1 and 2 reverse the phase or polarity of the signal, then amplifier 3 must not introduce a polarity reversal. This can be seen with reference to Figure 16. Let the signal

be a 200-percent bandwidth signal or a video pulse of positive polarity at the input of Figure 15, like that shown in Figure 16(a).

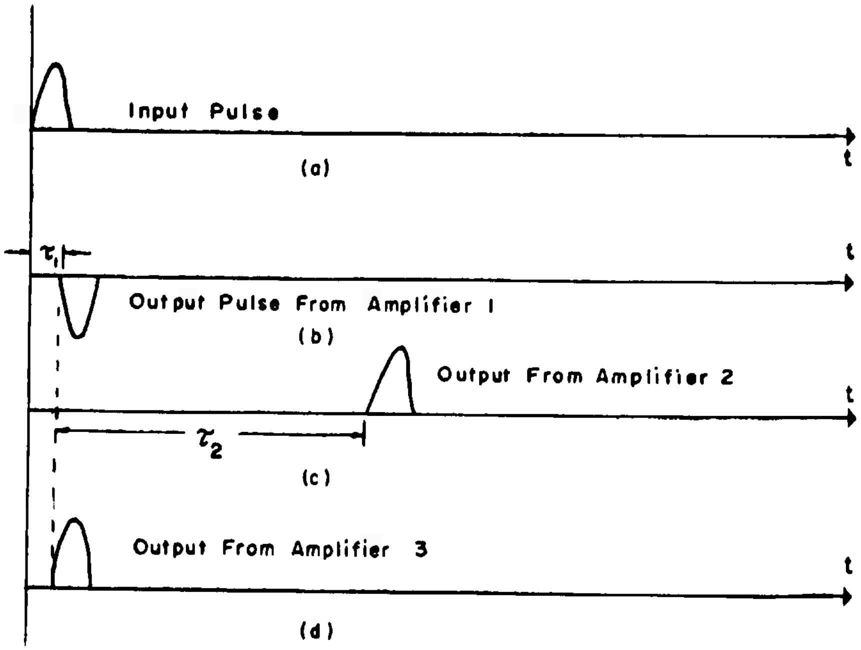

Figure 16. Effect of Signal Path Polarity in Single-Bit Digital Delay Line

After this pulse passes through the first amplifier, its polarity is reversed as shown in Figure 16(b). If the second amplifier is of the same type, the signal polarity is reversed back to its original condition, as shown in Figure 16(c). Note that τ_1 is the propagation delay through amplifier 1; τ_2 is the delay through both the delay media and amplifier 2. Such polarity reversals are obtained with the common emitter transistor amplifier configuration.

When the signal is passed through signal path 2, its output must have the same polarity as path 1 had. This is shown in Figure 16(d). In this example, a grounded base amplifier could be used for amplifier 3 since it does not affect the signal polarity. Wideband reversing transformers could also be used [3].

The maximum phase and amplitude ripple or variation across the band for a digital delay system will be specified. Since the variation in each bit of the system can add at points across the band to produce a larger variation for the system, the specifications on each bit must be more rigid than for the overall system. If the system amplitude variation is given by X db's and the system is to have N bits, then each bit must be flat, X/N db. The same is true for the phase response; however, it is much more difficult to calculate the effect on phase.

In the two-bit delay unit described here, it was desired to hold the ripple to better than one db across the band. This requires a maximum of a 0.5 db ripple per bit.

Wideband transistor amplifiers can be built flat to well below 0.5 db [4] without much trouble. Therefore, most of the ripple can be expected to result from the delay media itself.

Generally, this is due to improper termination or poor connectors as discussed in the preceding section. This ripple is reduced by introducing attenuation into the line, preferably at its input. The value of attenuation, α, is determined from equation (25) as,

$$\alpha^2 = \frac{(\sigma_{att} - 1)(\sigma + 1)}{(\sigma_{att} + 1)(\sigma - 1)}, \tag{26}$$

where σ_{att} is the desired ripple,

$$\sigma_{att} = 0.5 \text{ db} = 1.06.$$

The value of σ, the VSWR without attenuation, must be measured.

Amplifiers 1 and 2 of Figure 15 were constructed to measure the SWR, σ, or gain variation when the delay line was terminated into an amplifier. The circuit diagram of the amplifiers used for amplifiers 1 and 2 is shown in Figure 17.

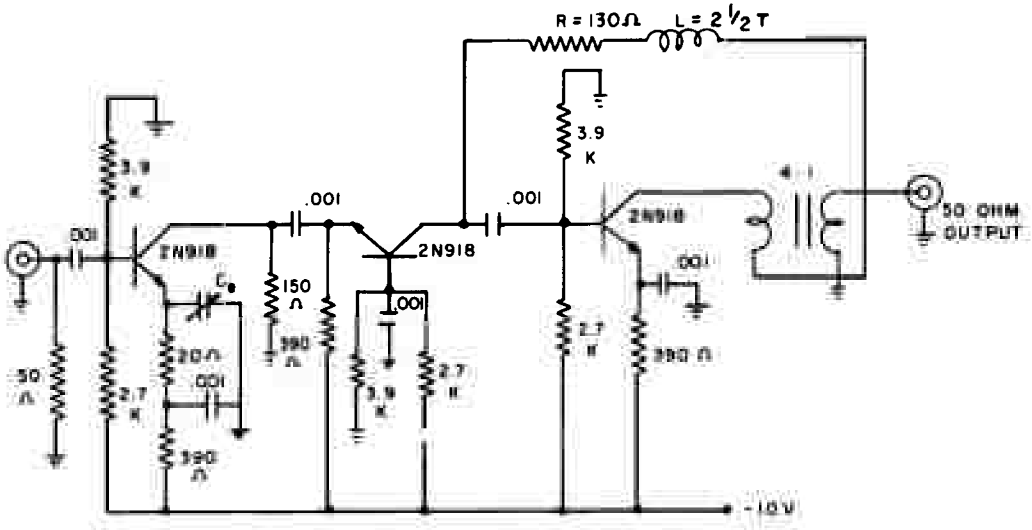

Figure 17. Circuit of Wideband Transistor Amplifier Referred to as the BABB (Basic Amplifier Building Block)

The phase and amplitude response of one amplifier is shown in Figure 18.

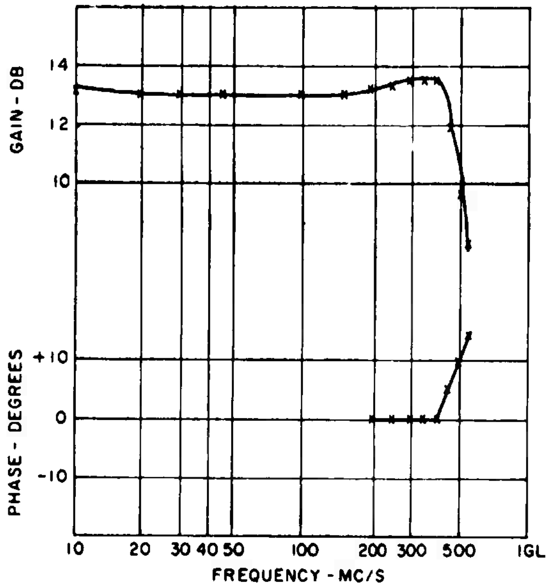

Figure 18. Amplitude and Phase Response For
BABB Amplifier of Figure 17

Two such identical amplifiers were connected through a three-foot length of RG-58A, 51-ohm coaxial cable. Note that the input to the amplifier is shunted by a 51-ohm resistor. Since the input impedance to the transistor amplifier is high compared to 51 ohms at low frequencies, this provides proper termination for the connected lines.

With no attenuation in the coaxial line, the two-cascaded amplifier gain response is shown in Figure 19(A). From this response, the gain is seen to fluctuate about 6.5 db. Therefore,

$$\sigma = 6.5 \text{ db} = 2.11. \tag{27}$$

This gain variation was not due to interstage interaction. Both amplifiers were cascaded directly and found to be flat to within about 0.5 db. See reference [4] for design details of these amplifiers.

Substituting the values from equations (26) and (27) into equation (25) yields a required attenuation of

$$\alpha = 13.6 \text{ db}$$

to be placed in the coaxial in order to reduce the gain fluctuations to 0.5 db.

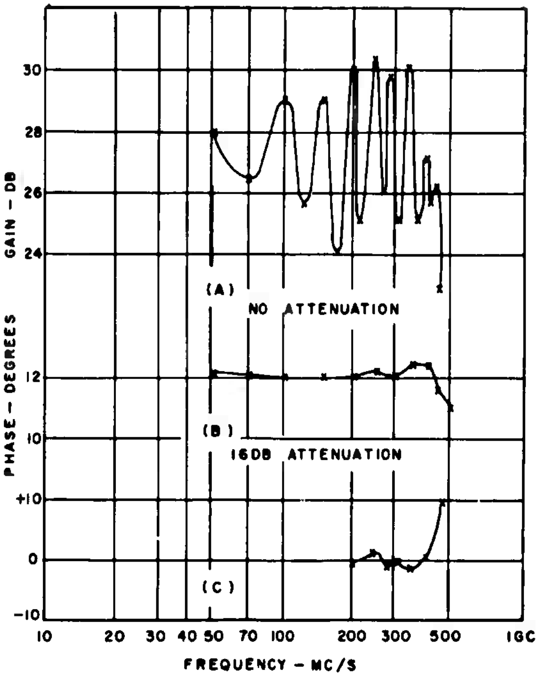

Figure 19. Wideband Cascaded Amplifier Response For Different Attenuations (3 Ft. Coax Between Amplifiers)

To provide a better input match at the second amplifier and overcome some of the lead length between connector and circuit, it was decided to split the attenuation. Part of it was placed at the input to amplifier 2 and the remainder placed at the input to the delay coaxial line. To ensure sufficient ripple reduction, a total of 16 db attenuation was used. It was divided with 6 db between the delay line and amplifier 2, and 10 db between amplifier 1 and the input to the delay line.

To reduce this effect, "tee" pads were constructed of 1/4-watt resistors and wired directly into the circuit. Their frequency response was checked with that of General Radio coaxial attenuators and found to be identical. The circuit of these "tee" pads is shown in Figure 20 alon with a block diagram of how they were located. The response of Figure 19(B) resulted.

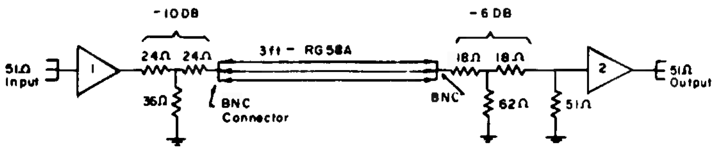

Figure 20. Attenuator and Amplifier Configuration

The variation is seen to have been reduced to the desired 0.5 db level. The peak at the high end is actually due more to a slight peak in the amplifier response. Figure 19(C) shows the phase response for this latter case. The phase measuring equipment available went down to only 200 mc/s.

The better the delay line termination, the less attenuation required. If the bandwidth is extremely small compared to the delay line, a point can be reached where the gain variation will begin to decrease and less attenuation will be required. Generally, however, when this point is reached, time delay steering is no longer required in an array antenna.

G. Isolation Requirements

With reference to Figure 1 if the input signal is passed through path 1 with path 2 switches open, the output frequency response will exhibit ripples if the isolation through path 2 is not sufficient. Lack of sufficient isolation can be caused by leakage through the open switches or by coupling between input and output due to the improper physical location of components. In fact, parts of path 1 could couple into the output of path 2. In practice, it was found necessary to shield the two paths.

To determine how much isolation is required, we can write the maximum and minimum output signal voltage as

$$V_1 + V_2 = V_{max}$$

and (28)

$$V_1 - V_2 = V_{min}$$

V_1 is the signal voltage at the output of path 1. V_2 is the leakage through path 2. At certain frequencies, the two signals will add to produce a maximum and at other frequencies they subtract to produce a minimum. The ratio, σ_β will then give a measure of the isolation effects in a manner similar to the VSWR.

$$\sigma_\beta = \frac{V_{max}}{V_{min}} = \frac{V_1 + V_2}{V_1 - V_2} \quad . \tag{29}$$

If we denote the isolation through the off path by β, the

$$\sigma_\beta = \frac{(1 + \beta)}{(1 - \beta)} \tag{30}$$

or the isolation required to reduce the ripple from this effect below the level σ_β is given by

$$\beta = \frac{\sigma_\beta - 1}{\sigma_\beta + 1} \quad . \tag{31}$$

This expression is plotted in Figure 21. The phase will also be affected by the lack of proper isolation.

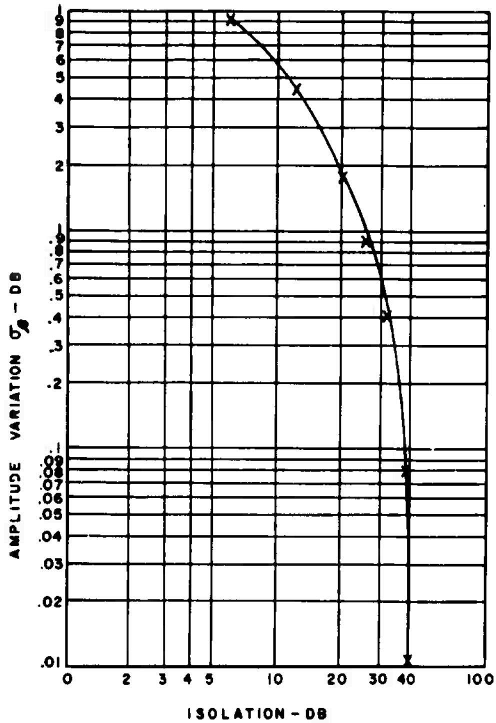

Figure 21. Feedthrough Isolation Versus Amplitude Variation

For an amplitude variation of less than 0. 1 db, the minimum isolation through each path must be 40 db.

When a single-stage transistor amplifier is turned off, it produces an isolation of 20 db. To increase this isolation, a convenient trick is to place a diode in series with the collector. The diode should have a low dynamic impedance. When the transistor is turned off, the dynamic impedance of the diode increases, thus increasing the isolation. A small reverse bias will help by decreasing the effective diode capacitance. Isolations greater than 40 db have been obtained from a single transistor amplifier by this technique.

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II. CIRCUIT DESCRIPTION OF TWO-BIT DIGITAL DELAY LINE

A. Description of Block Diagram

Many different amplifier configurations are possible in forming either a single or double bit digital delay line. The approach taken, after considering many alternatives, was to design two bits as an integral unit. The unit basic configuration is shown in Figure 22.

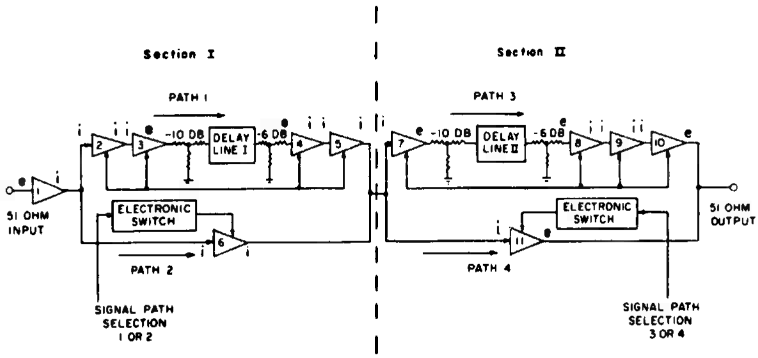


Figure 22. Block Diagram of Two-Bit Digital Delay Line

As determined by the electronic switch which applies power to the proper amplifiers, the input signal is passed through the first delay line, path 1, by turning amplifiers 2, 3, 4, and 5 on and amplifier 6 off. The reverse power conditions result in the signal passing through path 2. The same procedure is followed at the second bit, where either path 3 or 4 can be selected.

The delay lines are lengths of 51-ohm, RG-58A coaxial cable. No attempt was made to use high-quality cable since the only object was to prove feasibility.

The need for the attenuators and the determination of their value was discussed in the preceding section.

As discussed in a previous report by this author on the design of cascading wideband amplifiers [4], it is of utmost importance that the output of each stage be selected in a manner that requires minimum adjustments. Furthermore, it is important that the input characteristics of amplifier 2 and 6 and 7 and 11 be identical. This results in minimum impedance changes as the signal path is changed. Also, the output drive characteristics of amplifiers 5 and 6, and 10 and 11 must be identical. This does not say that 5 and 10 be identical.

The basic amplifier building block unit is that shown in Figure 23. The schematic diagram of this three-amplifier chain is shown in Figure 17. Its phase and amplitude response is shown in Figure 18. The basic amplifier configuration uses an emitter feedback input stage that has a high input impedance relative to 51 ohms. The input is shunted by a 51-ohm resistor to provide proper termination

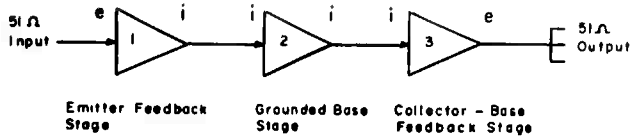


Figure 23. Basic Amplifier Building Block (BABB)

for the driving source. The output characteristics of this stage resemble a current generator and as such are ideally suited to drive the low input impedance of the grounded base amplifier. Due to the extremely low input impedance of the second stage, the power gain of the first amplifier is slightly above unity. The primary purpose of amplifier 1 is to provide an impedance transformation with no loss in gain and with minimum interstage interaction. See reference [4] for a complete discussion of this configuration. The output characteristics of the grounded emitter stage again resemble a current generator and can drive the collector-base feedback amplifier with minimum interaction. The input to amplifier 3 is strictly current sensitive. Its output has a low driving source impedance and thus appears more like a voltage source.

It might be asked why amplifier 2 should be used at all since it appears to contribute little. This is discussed in detail in reference [4]; however, a brief explanation is given here. The prime objective in building wideband cascaded stages is to minimize interstage feedback and resulting interaction. This is best obtained by driving a low impedance from a high impedance and a high from a low impedance source. This does not by any means yield maximum power transfer, but it does provide reasonable gain and minimum adjustment time.

The input to amplifier 2 is much lower than to amplifier 3; also the output impedance of amplifier 2 is much greater than that of amplifier 1. While the output impedance of amplifier 1 is not high enough to drive amplifier 3 without interaction, it is however high enough to drive amplifier 2; the output of amplifier 2 is quite high enough to drive amplifier 3.

A number of identical amplifiers of this configuration were built and tested. Only two adjustments were required to yield flat (0.5 db) response. The resistor in the feedback loop of amplifier 3 (See Figure 17) was adjusted to give the desired low frequency gain. The inductor was next adjusted to provide a flat high frequency response. In each case there was no evidence of interaction between stages. Interaction shows up as peaks and dips within the bandpass.

The symbols at the input and output of each amplifier in Figure 22 indicate the characteristic of that part. An "e" indicates that the input is voltage sensitive and should be driven from a voltage source. At the output, it indicates that the driving source resembles a voltage generator. The "i" indicates a current source or drive.

When cascading amplifier stages, it is important that connected terminals or ports have the same symbol, as shown in Figure 22.

In selecting the individual design for the amplifiers shown in Figure 22, the Basic Amplifier Building Block (BABB) of Figure 23 is followed.

Following from the input through path 1, the three-stage BABB is used for amplifiers 1, 2, and 3. That is, amplifier 1 of Figure 22 is identical to amplifier 1 of Figure 23. The same is true for amplifiers 2 and 3 in the two figures.

In order to minimize level changes due to impedance variations when the signal is switched from one path to the other, it is necessary that the input stage to both paths be identical. The same is true of the output stages of each path. Therefore, amplifiers 2 and 6 are identical grounded base amplifiers as indicated in Figure 23.

The second BABB consisted of amplifiers 4, 5, and 7, or 11. Note again that amplifiers 7 and 11 must be identical. However, only one is operative at a time. Note also that amplifiers 6 and 5 must be identical since they are both output stages of each signal path. Again, only one of these amplifiers is operative at a time. Comparing Figure 22 with Figure 23, amplifier 4 must be an emitter feedback amplifier. This configuration is dictated by the fact that it is driven from a 51-ohm voltage source. Amplifiers 5 and 6 are both grounded base amplifiers. Amplifiers 7 and 11 are collector-base feedback stages. Their output characteristics resemble voltage sources and amplifier 7 is ideal for driving the delay line. Since amplifier 11 drives the output of the unit from path 4, an identical amplifier must drive the units' output from path 3. This requires that amplifiers 8, 9, and 10 be the BABB.

Note that no matter which pair of signal paths is selected, the signal always passes through one, two, or three complete BABB's. If path 2 - 4 is selected, amplifiers 1, 6, and 11 make up one BABB. For path 2 - 3, amplifiers 1, 6, and 7 form one BABB, while 8, 9, and 10 form another. Paths 1 - 4 and 1 - 3 form two and three BABB's, respectively. Although the two delay paths have a different amplifier arrangement, the same number of stages are used.

Combining all amplifiers in this manner yields a smooth noninteracting signal flow through any path combination while at the same time providing an amplifier design that is reproducible and requires a minimum of adjustments. This last factor is most important when such a device is to be reproduced.

A number of these two-bit digital lines could be cascaded to yield a four, eight, or more bit system. Although only a single unit like that shown in Figure 22 was built, no interaction should be encountered in cascading identical units.

When the signal is passed through path 1, the isolation provided by the single amplifiers 6 and 11 is not sufficient in itself to prevent significant amplitude variation. Amplifier 6 is a grounded base amplifier. It produces about 20 db of isolation when biased off. The insertion of a low dynamic impedance, germanium diode in series with the collector increases the stage isolation to above 40 db. When the amplifier is turned on, the collector current automatically biases the diode on.

Amplifier 11 is a collector-base feedback amplifier and care must be taken as to where the diode is placed.

The isolation provided through the delay paths is then quite sufficient in itself. With three of the four amplifiers providing 20 db each (the collector-base feedback does not provide much isolation), plus 16 db of attenuation, the isolation is well over the 40 db required to limit the amplitude variation to less than 0.1 db (See Figure 21).

B. Description of Circuit Diagram

The circuit diagram for the two-bit digital delay line is shown in Figure 24. The numbers above each amplifier stage correspond to the amplifiers in the block diagram of Figure 22. All NPN transistors are 2N918. Most of these transistors had minimum current gain bandwidth products, f_T, of 750 mc/s. A few were slightly below this. Consequently, the amplifiers using these transistors did not have quite as good high frequency response as the others.

Amplifiers 1, 2, and 3 are identical to Figure 17. The transformer "T" in the output of the third stage is a wideband 4:1 impedance transformer [3]. It is wound on a 0.08 ID toroid of high permeability. The primary and secondary windings are formed by twisting two pieces of #30 enamel-covered wire together and then placing two turns on the toroid. This transformer is discussed in more detail in Section VI (C) under components.

The amplifier stages are adjusted by driving with a sweep generator (Jerrold 900B was used) and adjusting the low frequency gain to the desired value with the resistor, R_{11}, located in the feedback loop of the third stage, Q_3. The high frequency response is adjusted for maximum flatness with the inductor L. In some cases the transformer inductance was sufficient.

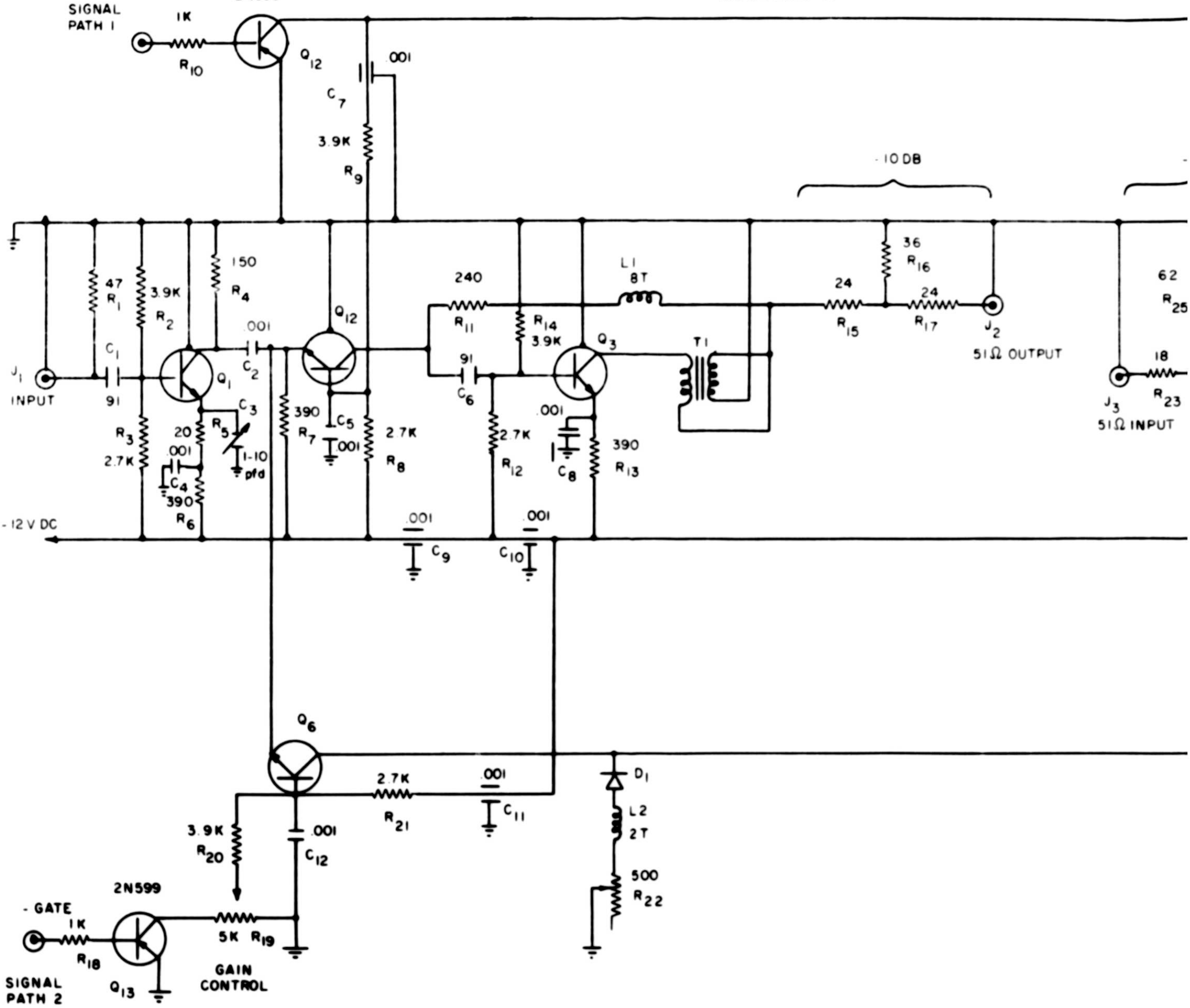
All amplifiers are laid out in such manner as to minimize lead lengths. The layout used here is shown in Figure 25. All coaxial connectors are BNC types. The input and output terminals are designated by J_1 and J_6. RG-58A coaxial cable was used for the delay media and was connected to the circuit by connectors J_2 and J_3 in the first section and J_4 and J_5 in the second section. This provided an easy way to change delays as well as to adjust each BABB.

A diode, D_2 is placed in the collector of amplifier Q_6 to provide adequate isolation when the stage is gated off. Diode D_3 is placed in the collector of amplifiers Q_5 mainly for symmetry; that is, to help keep the driving impedance identical. The series inductor, resistor, and diode-L_2, R_{22} and D_1- in the collector of Q_6 is to reduce the gain of the amplifier by about 6 db. The gain adjust control, R_{19}, only provides a fine adjustment.

The diodes at the input to amplifiers Q_7 and Q_{11} serve to isolate or disconnect the feedback impedance of the off amplifiers from the input of the on stage. Although the amplifier is off, the feedback impedance is still in the circuit and thus must be removed. These diodes, D_4 and D_5, are reverse or forward biased through resistors, R_{36} and R_{42}, respectively.

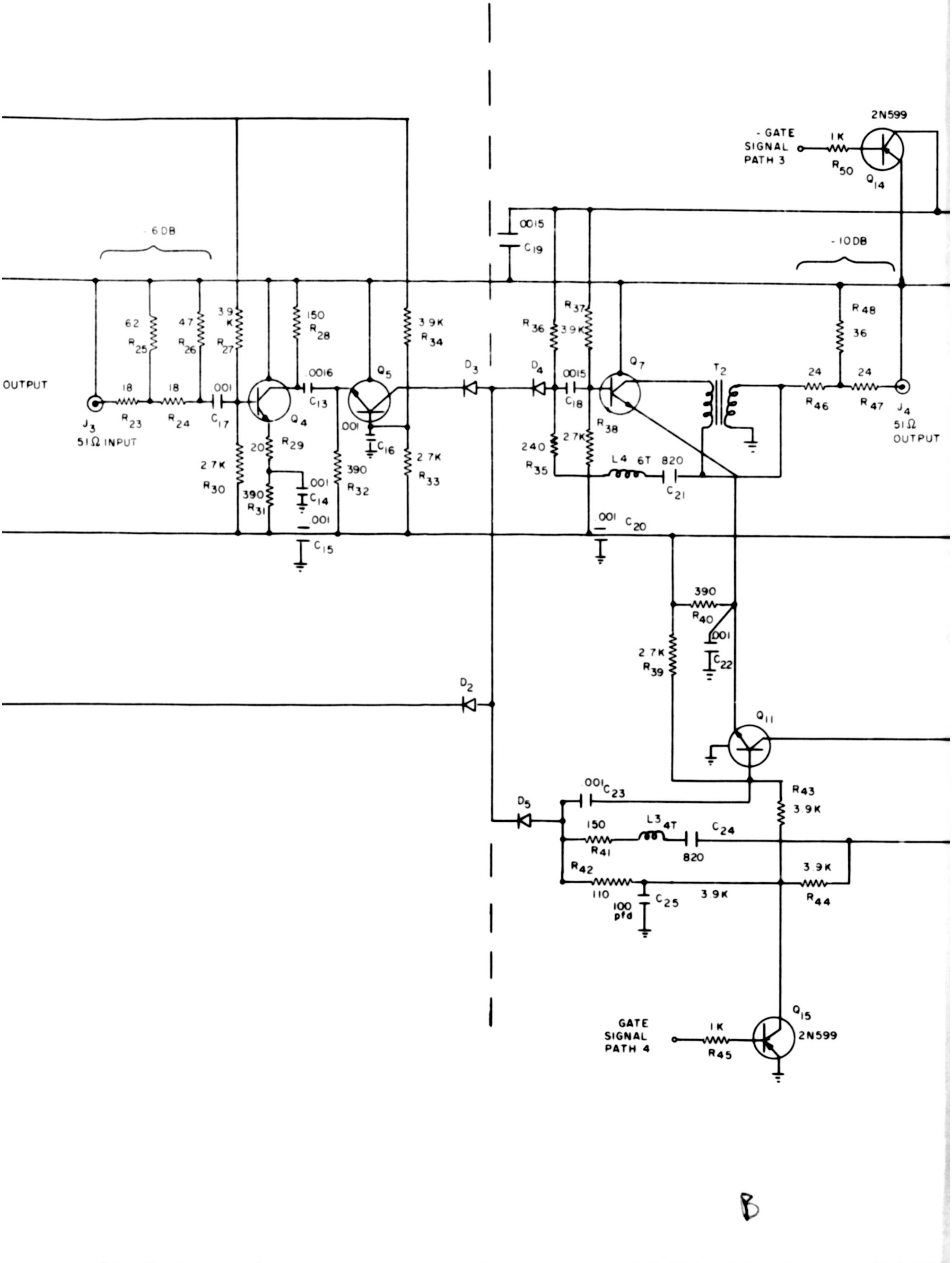
The output of both signal paths in Section II, amplifier Q_{10} and Q_{11}, drive a common wideband transformer, T_3. When the desired amplifier is turned on, its diode, D_8 or D_9, is automatically forward biased and the amplifier is connected to the transformer; the other diode is reverse biased. A small reverse bias (supplied through R_{66} and R_{67}) is applied to these diodes when the amplifier is off. This bias

SECTION I



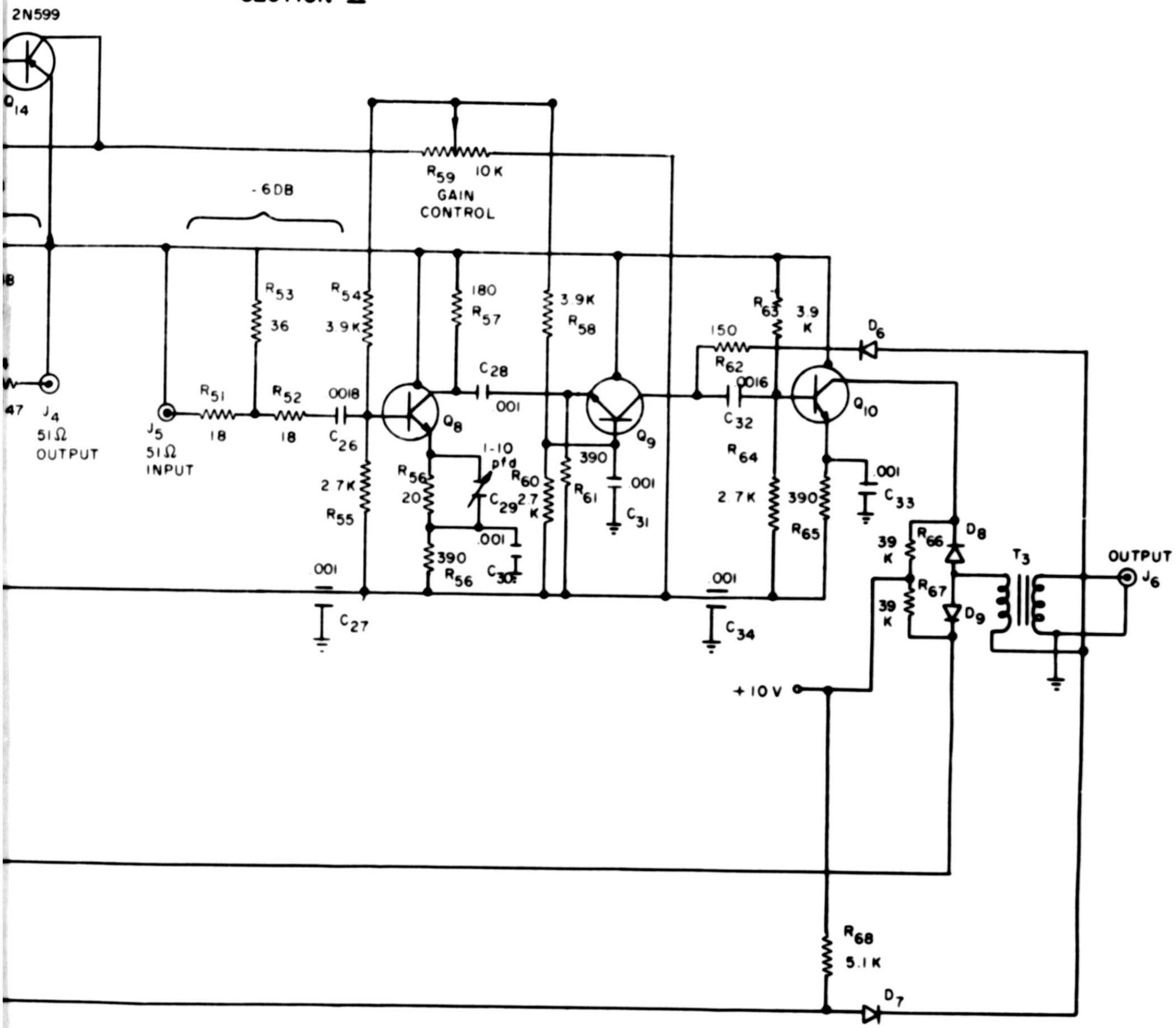
SIGNAL PATH I
2N599
1K
R10
Q12
.001
C7
3.9K
R9
-10 DB
36
R16
24
R15
24
R17
J2
51Ω OUTPUT
62
R25
18
R23
J3
51Ω INPUT
47
R1
3.9K
R2
150
R4
.001
C2
Q12
240
R11
L1
8T
R14
3.9K
Q3
T1
J1
INPUT
C1
91
Q1
C3
R5
1-10 pfd
20
R3
2.7K
.001
C4
390
R6
390
R7
C5
.001
2.7K
R8
91
C6
2.7K
R12
.001
C8
390
R13
-12 V DC
.001
C9
.001
C10
Q6
2.7K
R21
.001
C11
D1
L2
2T
500
R22
3.9K
R20
.001
C12
2N599
- GATE
1K
R18
5K
R19
GAIN CONTROL
SIGNAL PATH 2
Q13

A



OUTPUT
J3
51Ω INPUT
-6DB
62
R25
47
R26
18
R23
18
R24
.001
C17
3.9 K
R27
2.7K
R30
Q4
150
R28
.0016
C13
20
R29
390
R31
.001
C14
.001
C15
390
R32
Q5
.001
C16
3.9K
R34
2.7K
R33
D3
D2
D5
.0015
C19
D4
R36
R37
3.9K
.0015
C18
Q7
240
R35
2.7K
R38
L4 6T
820
C21
.001
C20
T2
-10DB
R48
36
24
R46
24
R47
J4
51Ω
OUTPUT
- GATE
SIGNAL
PATH 3
1K
R50
2N599
Q14
390
R40
.001
C22
2.7K
R39
Q11
.001
C23
R43
3.9K
150
R41
L3 4T
C24
820
R42
110
100
pfd
C25
3.9K
3.9K
R44
GATE
SIGNAL
PATH 4
1K
R45
Q15
2N599
B

SECTION II



(ALL PNP TRANSISTORS 2N599)
(ALL NPN TRANSISTORS 2N918)
L1 TO L4 COILS WOUND ON 1/2 WATT RESISTOR

Figure 24. Circuit for Two-Bit Wideband Digital Delay Line

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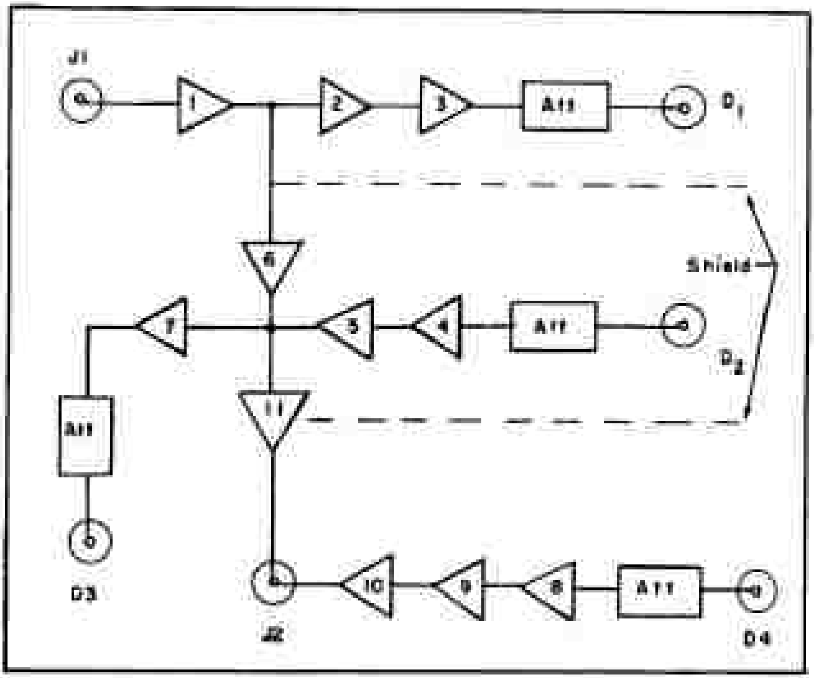

Figure 25. Physical Layout of Two-Bit Digital Delay Line

decreases the diode's junction capacitance which shunts the collector of the other amplifier and thus decreases its frequency response. Diodes D_6 and D_7 serve to disconnect the feedback impedance of amplifiers Q_{10} and Q_{11}.

Each amplifier is turned off by removing the base bias. The bias to several amplifiers within each path, which is provided through transistor switches Q_{12}, Q_{13}, Q_{14}, and Q_{15}, is driven from either a pulse generator or computer logic. The switch is turned on with a negative signal.

The primary power supply requirement is for -12 volts. The current required for each signal path combination is given below.

Signal Path	Current (Ma)	Power (Watts)
2-4	40	0.48
2-3	80	0.96
1-3	100	1.20
1-4	65	0.78

C. Incremental Time Delay Calculations

In order to calculate the incremental time delay or variation in delay between signal paths of both Section I and Section II (refer to Figure 22), we must first calculate

the delay through each path. Designating the delay through each signal path by subscript we write for the total delay between input and output through the various paths:

$$
\begin{aligned}
\tau_{1,3} &= \tau_{1,2,3} + \tau_I + \tau_{4,5,7} + \tau_{II} + \tau_{8,9,10} && \text{Path 1-3} \\
\tau_{1,4} &= \tau_{1,2,3} + \tau_I + \tau_{4,5,11} && \text{Path 1-4} \\
\tau_{2,3} &= \tau_{1,6,7} + \tau_{II} + \tau_{8,9,10} && \text{Path 2-3} \\
\tau_{2,4} &= \tau_{1,6,11} && \text{Path 2-4}
\end{aligned}
\tag{32}
$$

The delays $\tau_{1,2,3}$ etc., refer to the propagation delay through the BABB combination of amplifiers 1, 2, and 3. τ_I and τ_{II} refer to the delay introduced by the delay median.

To calculate the change in delay obtainable through Section I, when the signal is switched between path 1 and 2, we write:

$$
\begin{aligned}
\Delta\tau_I &= \tau_{1,4} - \tau_{2,4} = \tau_{1,3} - \tau_{2,3} \\
&= (\tau_{1,2,3} + \tau_{4,5,11} - \tau_{1,6,11}) + \tau_I \\
&= (\tau_{1,2,3} + \tau_{4,5,11} - \tau_{1,6,7}) + \tau_I \ .
\end{aligned}
\tag{33}
$$

The delay variation through Section II becomes:

$$
\begin{aligned}
\Delta\tau_{II} &= \tau_{1,3} - \tau_{1,4} = (\tau_{4,5,7} + \tau_{8,9,10} - \tau_{4,5,11}) + \tau_{II} \\
&= \tau_{2,3} - \tau_{2,4} = (\tau_{1,6,7} + \tau_{8,9,10} - \tau_{1,6,11}) + \tau_{II} \ .
\end{aligned}
\tag{34}
$$

If all of the BABB's are identical, then the delay, τ_{BABB}, through each will be the same. Therefore,

$$
\begin{aligned}
\Delta\tau_I &= \tau_{BABB} + \tau_I \\
\Delta\tau_{II} &= \tau_{BABB} + \tau_{II} \ .
\end{aligned}
\tag{35}
$$

The delays, τ, can be measured in a number of ways. The simplest and most accurate is to plot the phase versus frequency response of the BABB or delay line over its linear range. The slope of this line gives the propagation delay. That is,

$$\tau = \frac{d\phi}{d\omega} = \frac{\Delta\phi}{\Delta\omega} \ . \tag{36}$$

Here $\Delta\phi$ and $\Delta\omega$ must be in radians. Changing to degrees, this expression becomes

$$\tau = \frac{\Delta\phi^{o}}{2\pi \ 57.7 \, f} \ . \tag{37}$$

To determine the delay introduced by a coaxial cable, its relative velocity of propagation must be included. This data is generally given by the manufacturer or is found in tables [5]. If the cable length in feet is ℓ and its velocity of propagation relative to free space is ρ, the delay is given by

$$\tau_{cc} = 1.02\ \ell/\rho \text{ nanoseconds.} \tag{38}$$

Free space propagation is 1.02 nanosecond/1 ft.

D. Adjusting the Amplitude Response

The adjustment of the two-bit digital delay line is essentially the adjustment of the individual BABB's. Amplifiers 1, 2, and 3 are first adjusted by connecting a sweep generator to J_1 and the detector to J_2. The desired gain is obtained by adjusting R_{22} and maximum flatness by adjusting L_2. Amplifiers 4, 5, and 7 are next adjusted. The generator is connected to J_3 and the detector to J_4. At this point, connect the detector to J_6 and switch the signal through path 4 so that the response of amplifiers 4, 5, and 11 are viewed. Amplifier 11 is then adjusted. With amplifier 11 properly adjusted, the response of amplifiers 1, 6, and 11 should be flat. All adjustments should be made with gains adjusted to maximum. Amplifiers 8, 9, and 10 are then adjusted through connectors J_5 and J_6.

With the symmetry of all interconnecting stages and the lack of interstage feedback or interaction between signal paths, once the third amplifier of the BABB is adjusted, it can be switched with a negligible effect on the response.

As soon as these adjustments have been made, the delay cable lengths can be inserted. Driving the unit at J_1 from a sweep generator, with the detector at J_6, the response through paths 1 and 2 can be viewed. The first adjustment should be to equalize the path gains. Amplifier 6 is provided with a fine and coarse gain adjustment. The amount of adjustment will depend on the gain through path 1. A slightly high gain and flat response may be obtained by adjusting R_{22} and L_2. The gain control is then adjusted to equalize the gain through both paths. If the flatness of the two path responses differs, then the inductor of amplifier 3 should be adjusted to minimize this difference. The signal is next alternately switched through paths 3 and 4. The same adjustments are repeated. It was found necessary to reduce the gain of amplifiers 8, 9, and 10 because of the different gains of amplifiers 6 and 11. If good high frequency circuit components and techniques are used, there should be no difficulty in making the above adjustments.

Generally, the high frequency response of each BABB can be extended slightly by the addition of a small (1 to 10 pF) capacitor C_e at the emitter of the first amplifier. This adjustment is one of the last adjustments and must be made using the sweep circuit.

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III. TEST RESULTS OF TWO-BIT DIGITAL DELAY LINE

A. Amplitude and Phase Response

Each BABB combination was adjusted by the procedure outlined in the preceding section. The amplitude and phase response of each BABB in the two-bit system is shown in Figure 26 after the final adjustments were made.

Because several transistors had low values of f_T, the high frequency responses of several BABB's were poorer than expected. A flat response (0.5 db) to 400 mc/s or 3 db to 450 mc/s was desired. In adjusting C_e, the high frequency response of amplifiers 1, 2, and 3 were peaked to compensate for the undesired dropoff in the other amplifiers.

The phase measuring equipment started at 200 mc/s. The phase is seen to be quite linear up to 400 mc/s. The ±2 degrees of deviation is within the accuracy of the phase equipment over the band. The desired upper cutoff frequency of 450 mc/s shows a maximum deviation of only 5 degrees.

The slope of phase versus frequency over the linear range was measured at

$$\tau_{BABB} = \frac{1}{360}\,\frac{\Delta\phi}{\Delta f} = \frac{1}{360}\,\frac{10^{o}}{10\ mc/s} = 2.78 \text{ nanoseconds} \qquad (39)$$

for one BABB combination. The delay for each BABB was measured as follows:

$$\begin{aligned}
\tau_{1,\,2,\,3} &= 2.78 \text{ nanoseconds}\\
\tau_{4,\,5,\,7} &= 3.92 \quad ''\\
\tau_{4,\,5,\,11} &= 3.92 \quad ''\\
\tau_{8,\,9,\,11} &= 3.36 \quad ''\\
\tau_{1,\,6,\,11} &= 2.78 \quad ''\\
\tau_{1,\,6,\,7} &= 2.78 \quad ''
\end{aligned}$$

With a 16-ft. length of RG-58A in place of delay line I, Figure 22, and a 6-ft. length for delay line II, the phase and amplitude response of the complete two-bit digital delay unit is shown in Figure 27. The amplitude response is quite smooth up to about 350 mc/s and within the 1 db range to 400 mc/s. The variation above 400 mc/s is due to the use of transistors having an f_T below the desired, f_T, 750 mc/s, value.

If higher frequency transistors were used, i.e., f_T = 1500 mc/s, the bandwidth could be extended substantially. Here, however, the primary objective was to demonstrate the feasibility of this digital delay technique and not the maximum bandwidth obtainable. The transistors used for this experimental unit were 2N918's which cost six dollars each. With the state of the art in high frequency transistors improving at an ever-increasing rate, it would not be surprising if such a delay unit could be built in the S-or C-band at a cost of only 10 to 20 dollars per transistor.

The phase response for each delay path is seen to be quite linear up to 400 mc/s. At 450 mc/s, the deviation is seen to have increased to about 10 degrees.

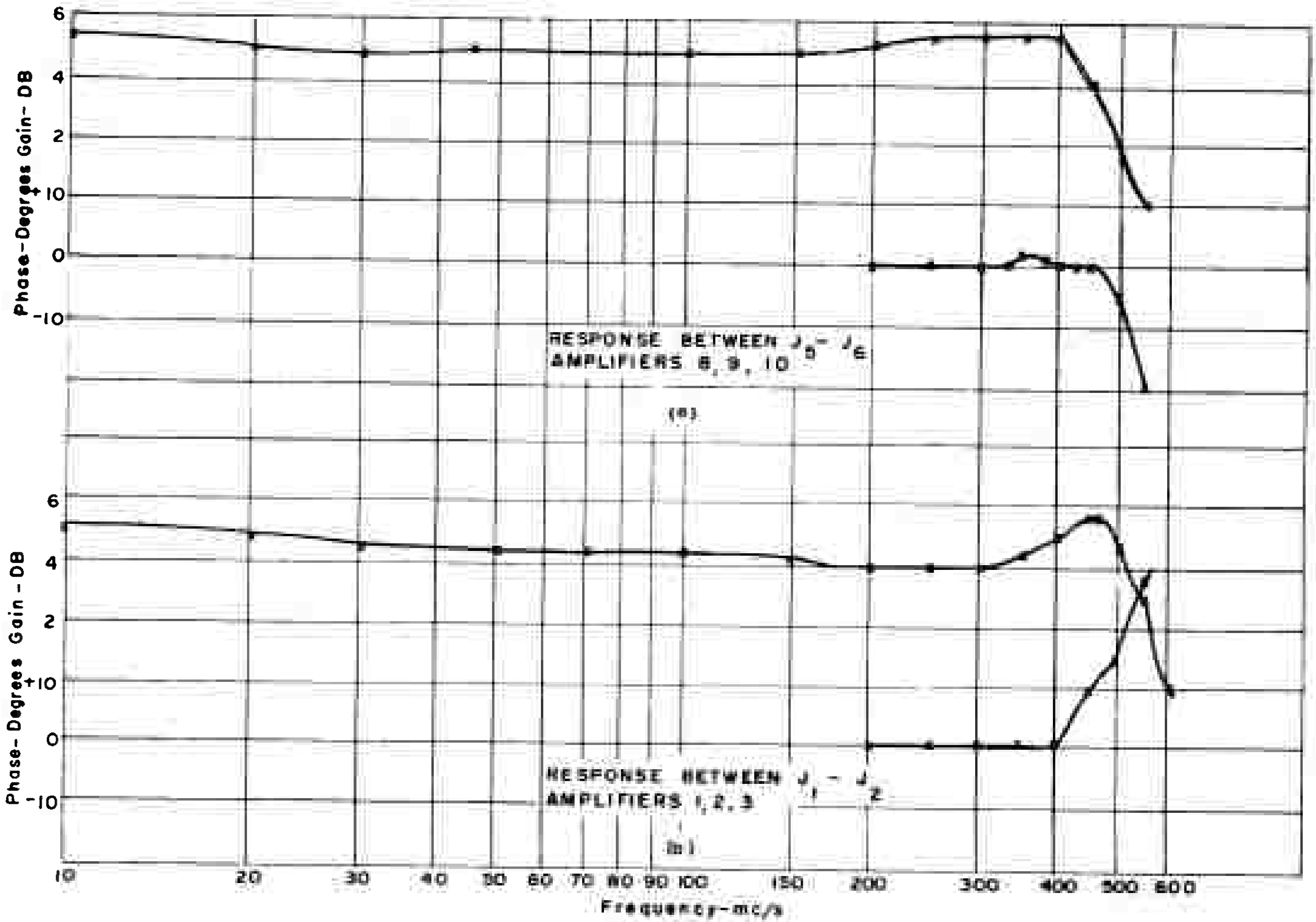


Figure 26. BABB Amplitude and Phase Response

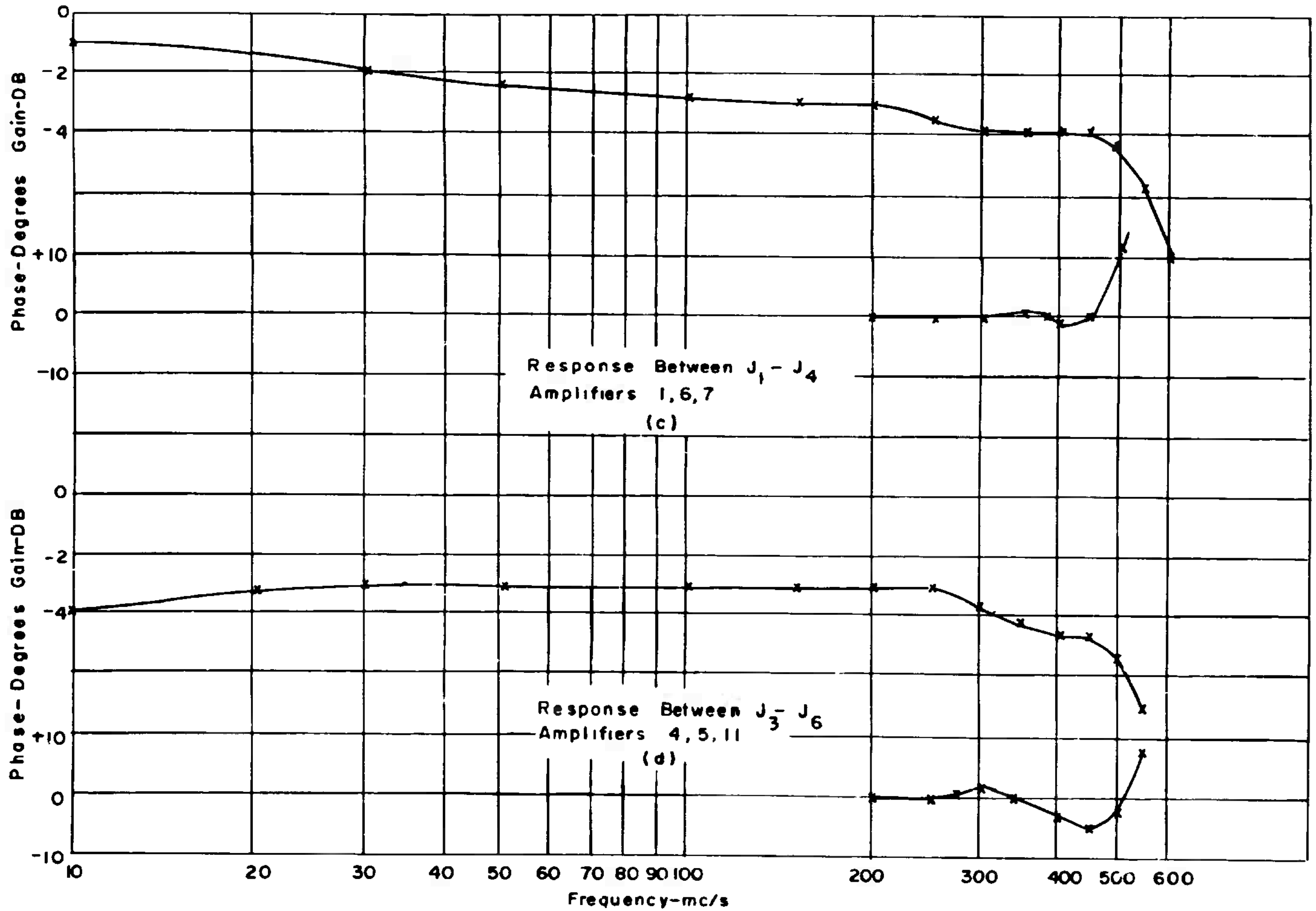


Figure 26. BABB Amplitude and Phase Response (continued)

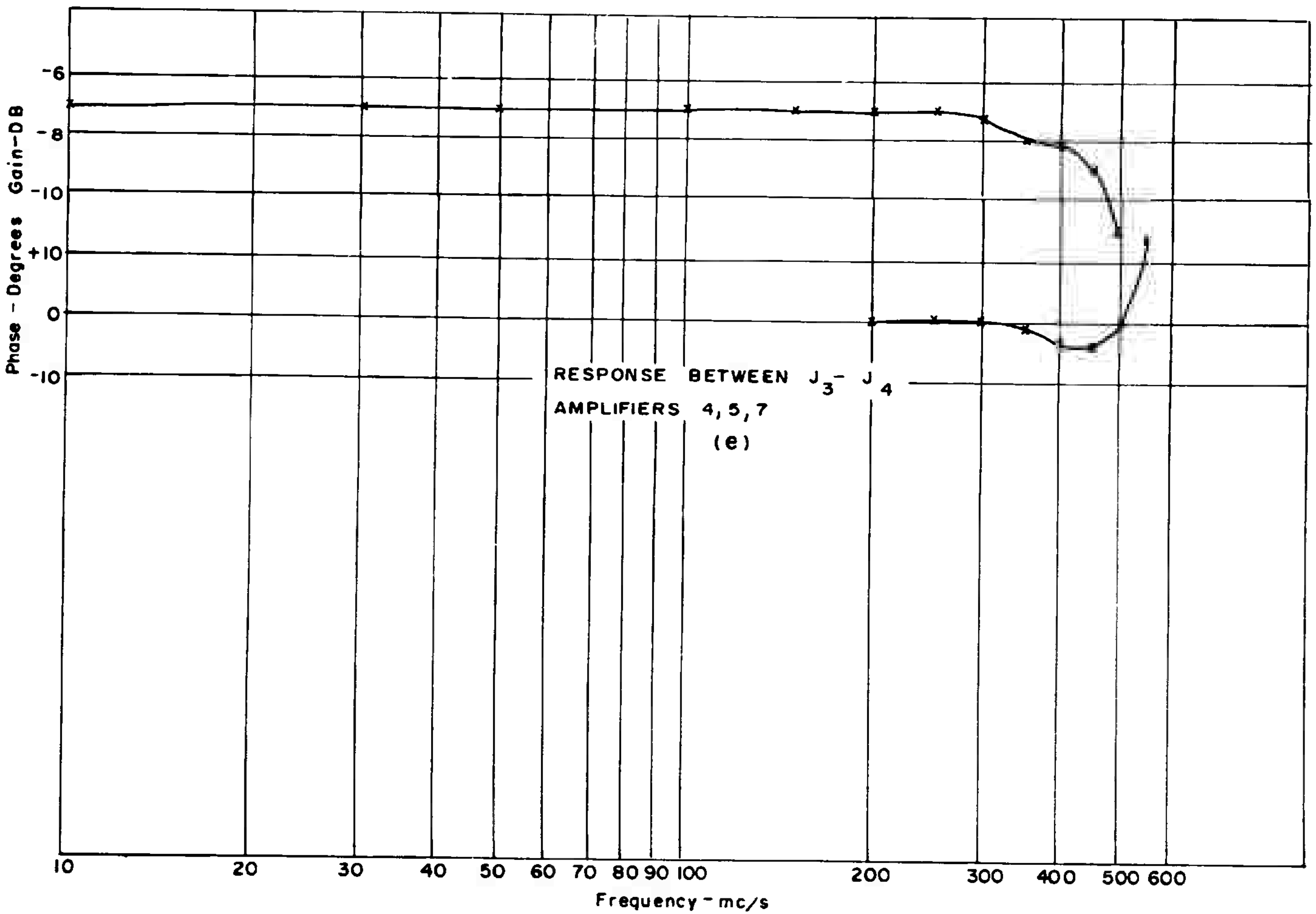


Figure 26. BABB Amplitude and Phase Response (continued)

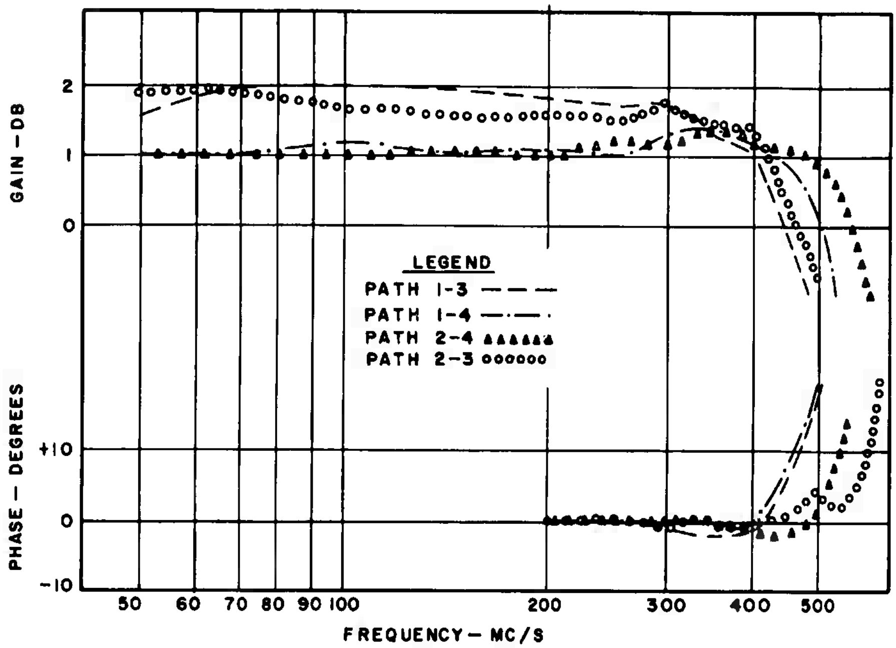


Figure 27. Amplitude and Phase Response of Two-Bit Delay System

B. Short Pulse and Time Delay Response

To demonstrate the variable delay characteristics of the two-bit digital delay, a short r-f pulse was passed through the unit. The output was viewed on a sampling oscilloscope that was synchronized to the input pulse. By turning the proper amplifiers on and off, the pulsed signal can be made to pass either through or around the delay paths of the two sections. The resultant signal delay is seen as a variation in pulse position on the oscilloscope. Generation of these short r-f pulse bursts is discussed in the next section of this report.

The delay median in Section I was a 16-foot length of RG-58A coaxial cable having a relative velocity of propagation, $\rho = 65.9\ \xi$. A 6-foot length of this cable was used in Section II. Substituting in equation (38)

$$\tau_I = 24.8 \text{ nanoseconds}$$
$$\tau_{II} = 9.3 \text{ nanoseconds} \qquad (40)$$

Determining the delays by the technique indicated by equation (32) gives

$$\tau_I = \frac{1}{360} \times \frac{90^o}{10\,\text{mc/s}} = 25 \text{ nanoseconds}$$
$$\tau_{II} = \frac{1}{360} \times \frac{33.3^o}{10\,\text{mc/s}} = 9.25 \text{ nanoseconds} \qquad (41)$$

Using these theoretical delays and the measured amplifier delays of equation (39), the variation in delay through the two sections (Figure 22) as given by equations (33) and (34) becomes

$$\begin{aligned} \Delta\tau_I &= 3.92 + 25.0 = 28.92 \text{ nanoseconds} \\ \Delta\tau_{II} &= 3.36 + 9.25 = 12.61 \text{ nanoseconds} \end{aligned} \tag{42}$$

Therefore, the four incremental time delays attainable with this two-bit unit are

$$0,\ 12.61,\ 28.92,\ 41.53 \text{ nanoseconds} \tag{43}$$

The first demonstration used 3-1/2 cycles of a 225 mc/s carrier as a signal. This corresponds to a 64.5 mc/s bandwidth or a 28.6 percent bandwidth signal. The input signal is shown in Figure 28(a). The scale is 10 nsec/Div. With the amplifiers of the minimum delay paths energized, path 2 - 4, the signal response of Figure 28(b) results. The indicated delay of about 4 nanoseconds does not correspond to the minimum unit delay. This position was arbitrarily set.

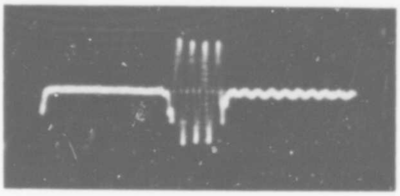
When the pulsed signal was switched through the delay path of Section II, i.e., path 2 - 3, Figure 28(c) resulted. The difference between this and Figure 28(b) gives the variation in delay for Section II, $\Delta\tau_{II}$. The experimental results are seen to be close to the theoretically calculated value of 12.61 nanoseconds given by equation (42).

Figure 28(d) shows the delay obtained when the signal was passed through the delay median of Section I with the delay of Section II bypassed, i.e., path 1 - 4. The resultant delay is close to the 28.92 nanoseconds calculated by equation (42).

With signal passing through both delay paths, Figure 28(e) resulted. This appears to be in error by about 3 nanoseconds as compared to the theoretical calculations. It is expected that the time scale of the scope was in error since it was not checked.

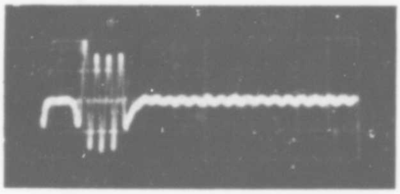
As a second demonstration, the wideband delay response of the two-bit delay unit was tested. Here the number of r-f carrier cycles was reduced to a one-half cycle. This corresponds to a 200 percent bandwidth signal and appears as a video pulse. With a carrier frequency of 225 mc/s, this corresponds to a 450 mc/s bandwidth signal. The input signal is seen in Figure 29(a). The bandwidth of this signal could be increased somewhat without suffering degradation when passed through the delay unit. Maximum signal-to-noise ratio is obtained when the bandpass of the delay unit and of the signal are matched by increasing the signal bandwidth; the signal bandwidth can be increased by raising its carrier frequency.

Figure 29(b, c, d, and e) show the 450 mc/s bandwidth signal for each of the four delay line path combinations. Here the time scale is 5 nsec/div. The only effect the delay unit appears to have had on the input pulse shape is to reduce the higher order harmonics.



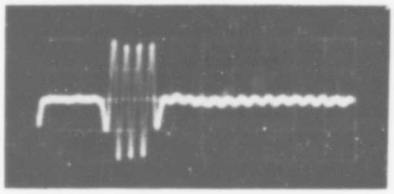
INPUT SIGNAL

(a)



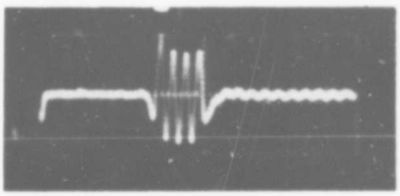
PATH 2-4

(b)



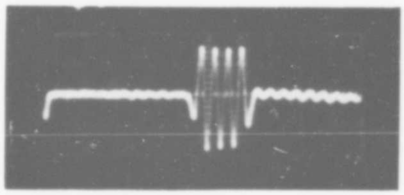
PATH 2-3

(c)



PATH 1-4

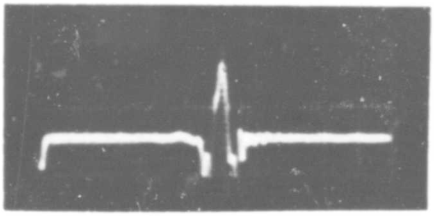
(d)



PATH 1-3

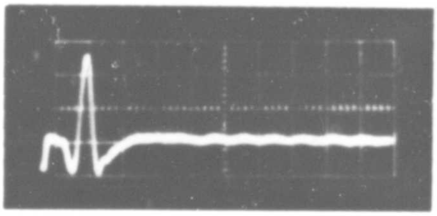
(e)

Figure 28. Time Delay Response to 65 mc/s Bandwidth Signal (10 nsec/div)



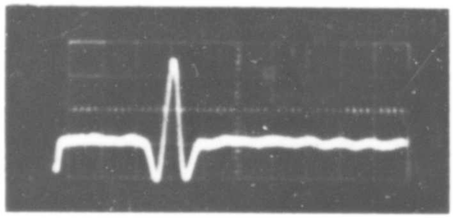
INPUT SIGNAL

(a)



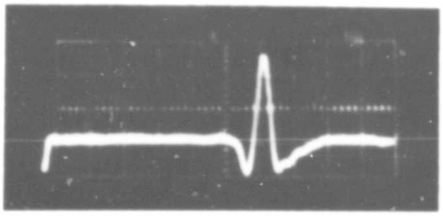
PATH 2 - 4

(b)



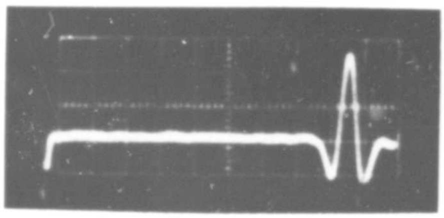
PATH 2 - 3

(c)



PATH 1 - 4

(d)



PATH 1 - 3

(e)

Figure 29. Time Delay Response to 450 mc/s Bandwidth Signal (5 nsec/div)

The two-bit digital delay line is shown in Figure 30. The actual circuitry is built on the left third of the board only. The two coils of coaxial cable form the two delay lines. The switches on the lower portion of the board are used to switch the bias to the transistors.

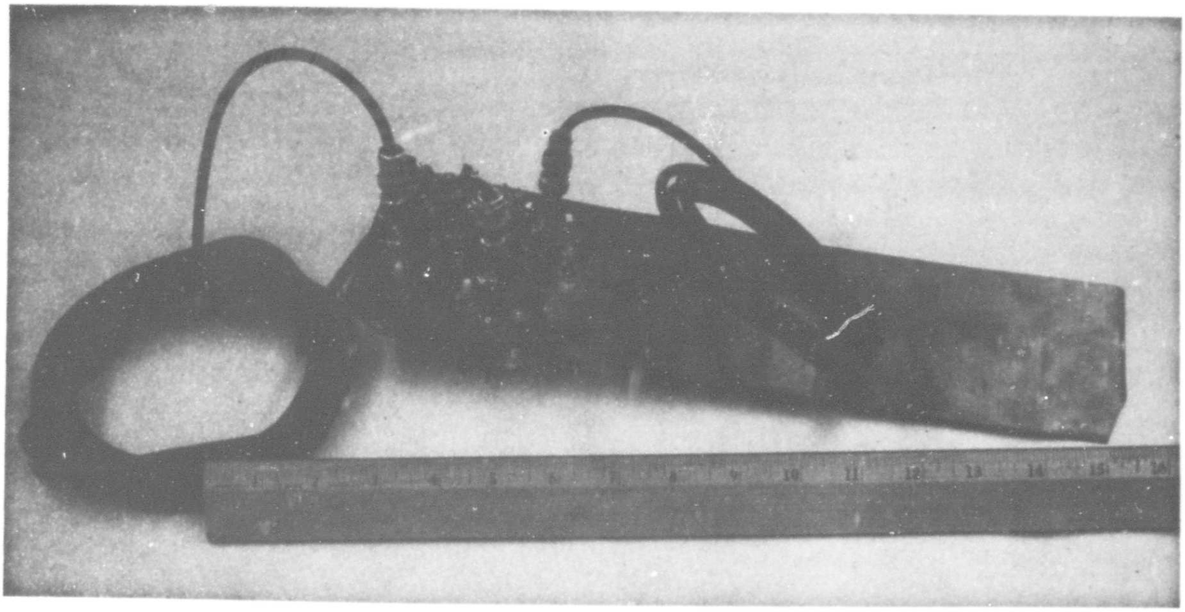


Figure 30. Photograph of Two-Bit Digital Delay Line

C. Reset of Switching Time

The reset of switching time required to switch the signal through alternate paths was measured at about 50 nanoseconds. The biasing transistor switches Q_{12}, Q_{13}, Q_{14}, and Q_{15} (Figure 24) change the biasing conditions required to turn the amplifiers either on or off. Normally, these transistors would be activated by computer logic gates.

To determine the switching time of each path, the undesired path was open-circuited. A CW signal applied at the input was monitored at the output of the delay line. The transistor bias switch was then connected to a Hewlett-Packard Model 215A, variable (1 to 100 nanoseconds) pulse width generator.

With proper drive to the switch, a pulsed CW waveform appeared from the delay line unit.

The turn on and off times were measured from the 100 percent points to what appeared to be complete absence of the CW signal. These times for both turn on and off were less than 50 nanoseconds. The switching transistor, 2N599, has an alpha cutoff of 12 mc/s which is probably the limiting factor in the switching time.

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IV. SHORT PULSE R-F GENERATOR

The function of the short pulse r-f source is to generate a pulsed CW carrier with adjustable pulse width. It was desired further that the initial phase of the CW pulsed carrier be the same from pulse to pulse. This does not mean that each pulse is coherent. By starting the phase of each r-f pulse at the same time, each cycle within the pulse can be viewed on an oscilloscope.

The circuit used to generate the desired pulsed r-f signal is shown in Figure 31.

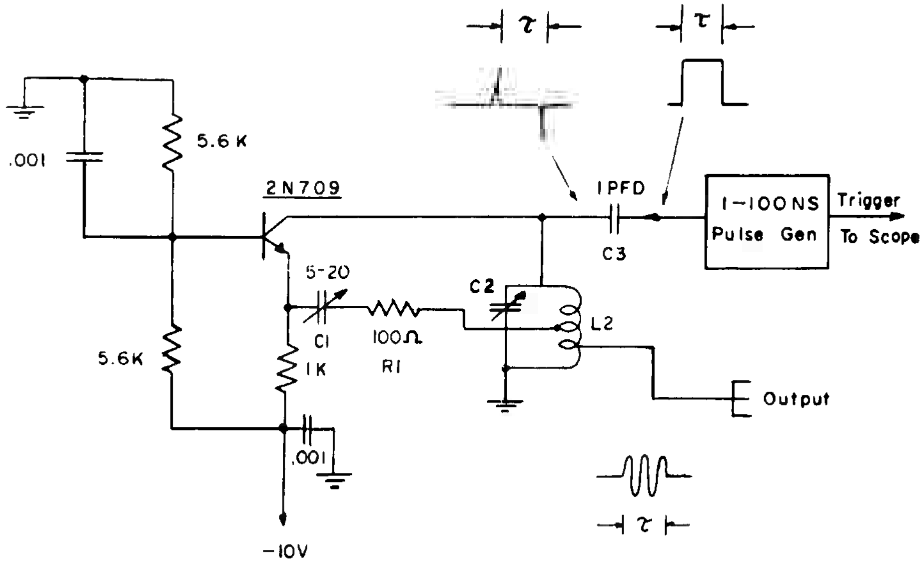

Figure 31. Diagram of Short Pulse Generator

The parallel tuned circuit, L_2 - C_2 is shock excited by the differentiated pulse from the pulse generator Model 215A. This square pulse is differentiated by C_3 which consists of a piece of wire located close to the coil L_2. The resulting differentiated pulse consists of two impulses of opposite polarity whose spacing is determined by the pulse width.

The initial impulse shock excites the parallel circuit which rings at its natural resonant frequency. The output from the resonant circuit is obtained by tapping the coil near the ground end so as not to load the circuit. If only the parallel circuit is used, the result will be an exponentially damped ringing as shown in Figure 32(a).

The second impulse from the differentiated trailing edge of the input pulse will produce a second damped ringing. The phase of this second shock-excited ringing will be of opposite phase to that of the first because the second impulse has an opposite polarity.

To overcome the losses in the circuit and eliminate the damped signal decay (produce a pulse of constant amplitude), it is necessary to introduce gain into the circuit. The signal is tapped off the coil and fed through R_1 and C_1 which are used

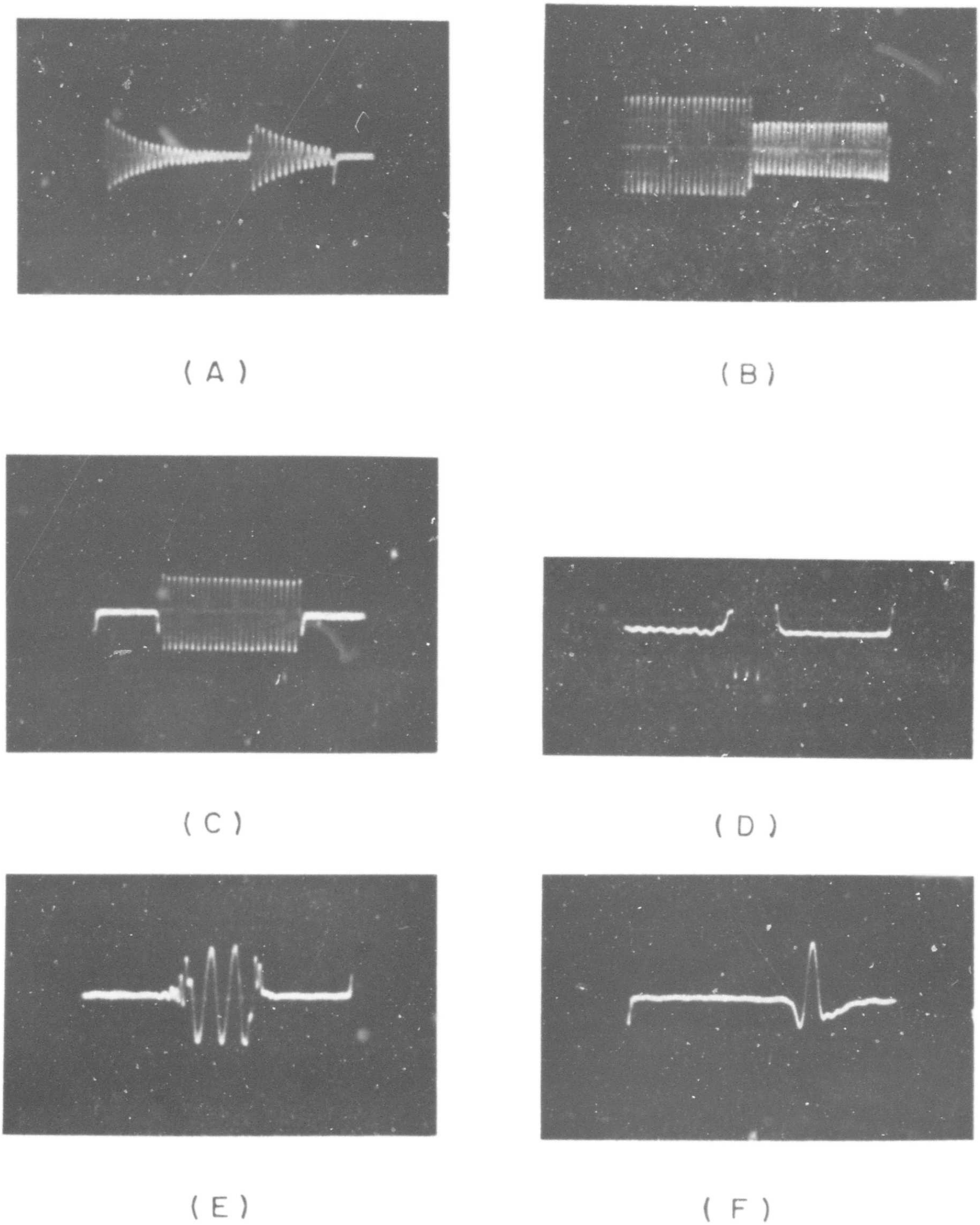

Figure 32. Waveforms From Short Pulse R-F Generator

to control the feedback to the emitter of the grounded base amplifier. The output of this amplifier is fed back to the parallel circuit. The gain is controlled by C_1 and adjusted to yield a loop gain as close to unity as possible without producing oscillation.

While viewing the shock-excited waveform on an oscilloscope, the gain is adjusted until minimum damping or sag is observed as shown in Figure 32(b). If the gain is increased further, the loop will break into undesired oscillation. The second half of Figure 32(b) is caused by the second impulse. The ringing produced here is timed so as to be in phase with the first and thus yield twice the original amplitude.

If the pulse width is either increased or decreased by a one-half r-f cycle, the two shock-excited waveforms will cancel to yield an r-f pulsed carrier width equal to the pulse generator pulse width as shown in Figure 32(c). By careful adjustment of the pulse width and feedback, this cancellation can be made to be nearly perfect. Failure to obtain perfect cancellation results in a slight amount of oscillation trailing the pulsed carrier as shown in Figure 32(d).

As the pulse width of the generator is reduced, the two excited waveforms (leading and trailing impulse) will alternately add and subtract. An even number of cycles results when the two waveforms cancel to produce the desired r-f pulse. Figure 32(e) shows the waveform when only 3 cycles are generated. Because of the finite rise time of the impulse, the initial and final cycles are attenuated. When the pulse width is reduced to 1 cycle as shown in Figure 32(f), the resultant waveform appears as only one-half cycle, or a 200 percent bandwidth signal.

It would be desirable to isolate the coil L_2 from the output by placing an amplifier between these two points, thereby preventing a variation in load from affecting the loop gain.

The sampling scope of a Hewlett-Packard Time Domain Reflectometer was used for viewing these short pulse waveforms. The pulse generator was triggered from the scope and the waveform fed to one of the signal input terminals. The other signal terminal was terminated.

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V. DESCRIPTION OF MEASUREMENT TECHNIQUES AND ASSOCIATED EQUIPMENT

A. Amplitude Response Measurements

The technique and equipment used to measure the amplitude response of the wideband amplifiers is shown in Figure 33. The test equipment setup is shown in Figure 34.

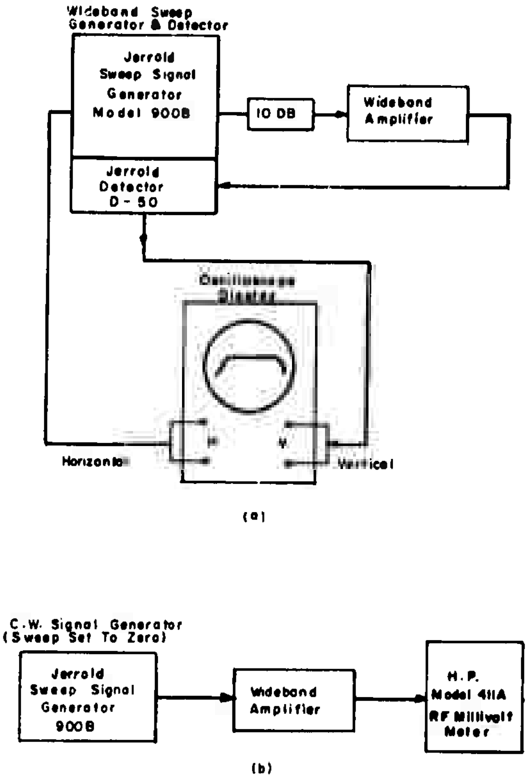


Figure 33. Amplitude Measurement Technique

To adjust the amplifier wideband amplitude response, the setup of Figure 33(a) was used. A Jerrold sweep generator Model 900B provided a swept CW signal over the desired band. This sweep generator has a built-in 50-ohm wideband detector, Model D-50. The input VSWR was well below 1.05. The detected output was displayed on an oscilloscope whose horizontal sweep was driven from the Jerrold sweep generator.

This generator has a wide- and narrowband sweep mode. For application here, only the wideband mode was used. In this mode, the generator is capable of sweeping from 0 to 400 mc/s in a single sweep with an internal crystal marker generator. The

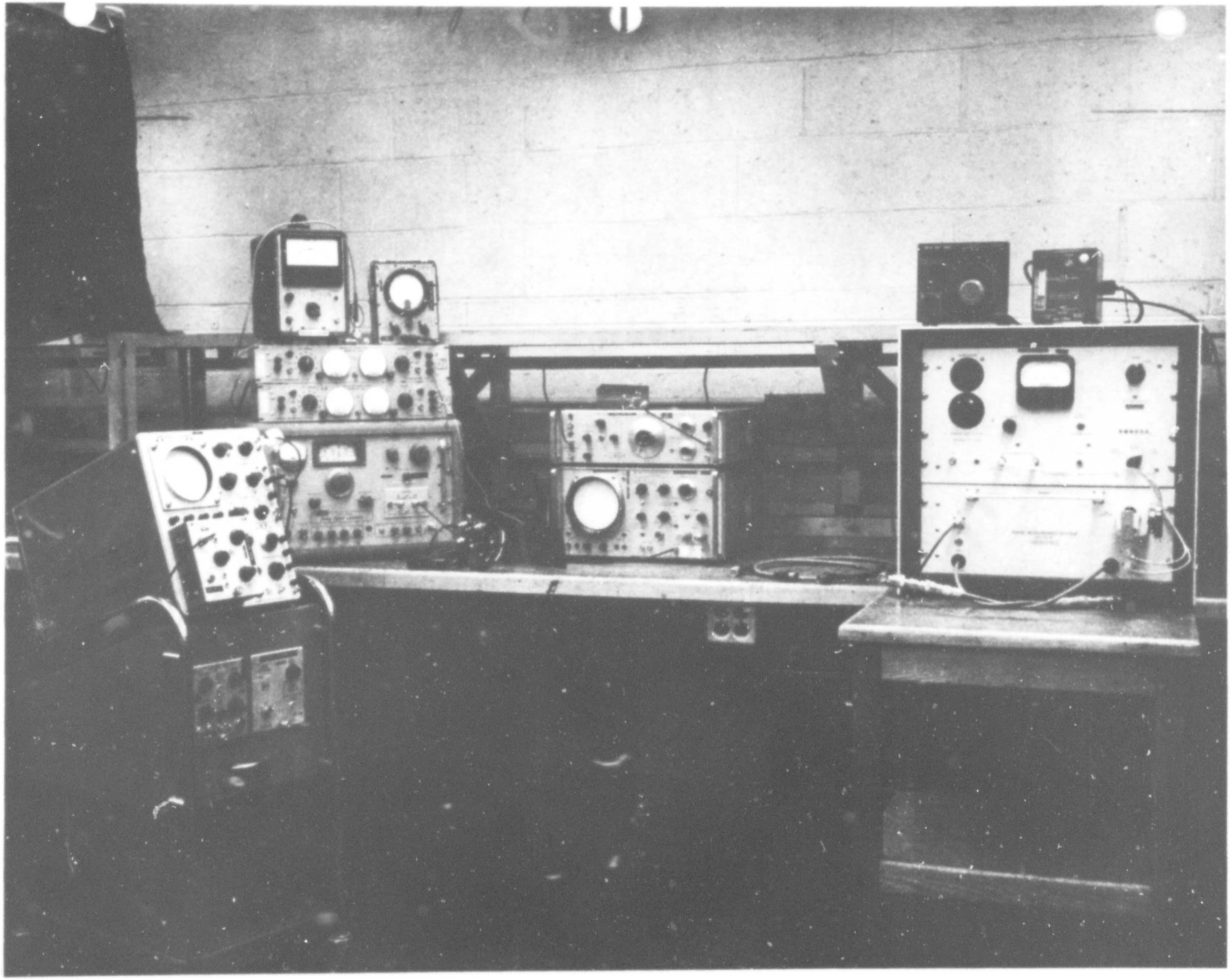


Figure 34. Photograph of Test Equipment

marker generator places marks on the sweep display at every 1, 10, and 100 mc/s intervals. Above 400 mc/s, the sweep width is only about 200 mc/s. However, the center frequency of this lower sweep width can be varied up to 1000 mc/s.

The output of this generator is dependent on proper termination. The inputs to all amplifiers were terminated with a 51-ohm resistor. Since at higher frequencies the transistor input impedance drops substantially, a 10-db pad was used between the generator and amplifier. The recommended coaxial cables (RG-58A and C) were used during each test.

When the generator is connected directly into the detector, the response of the instrument over the 400 mc/s sweep range is not flat. Over this frequency range, the amplitude varies by about 2 db. A photograph of this instrument response is shown in Figure 35.

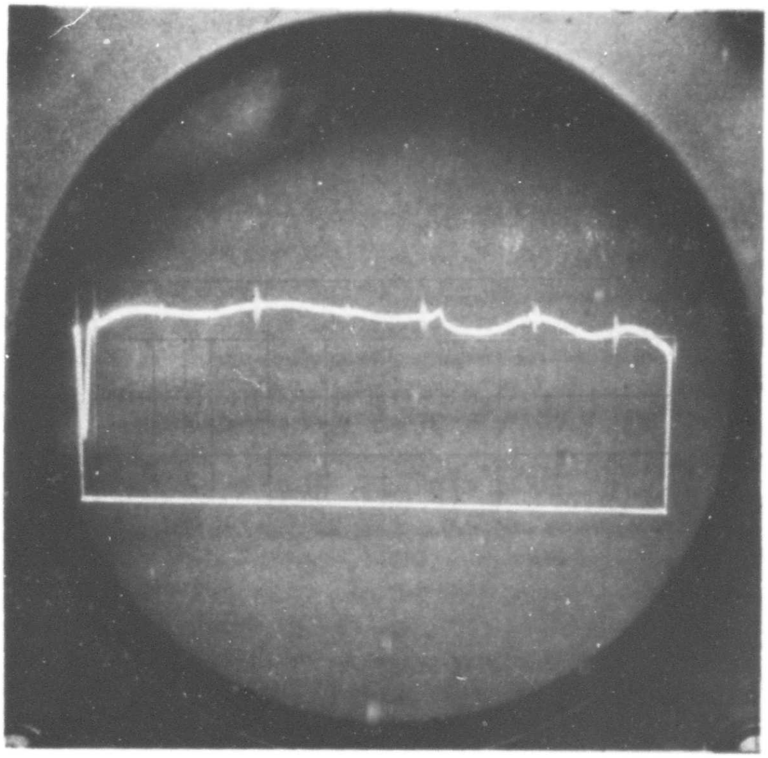


Figure 35. Photograph of Signal Generator Output

This variation is due to both ripples and a general downward slope with frequency. Above 400 mc/s, when a 200 mc/s wide sweep is used, the response is flat to within 0.5 db.

To measure the wide sweep in the 0 to 400 mc/s range, the generator response was traced on the scope display. The amplifier's response was then compared with this reference.

This measurement technique was used to adjust the wideband BABB amplifier response for maximum flatness. The final adjustment was that of C_e.

A more accurate technique was used to obtain the amplitude plots given in this report. For these measurements, the setup of Figure 33(b) was used. Here the sweep width of the generator was reduced to zero. The wideband amplifiers output was measured by a Hewlett-Packard Model 411A r-f millivoltmeter. This meter has a typical frequency response of 0.5 db from 0.5 to 1000 mc/s. Most amplitude response measurements were taken at 10, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500 and 550 mc/s. At each frequency, the generator's output level was first measured by removing the amplifier. The amplifier was then placed in the circuit and the gain determined.

The power supply used was an Electronic Measurements Company, Inc. Transistor Supply Model No. 212A which is variable from zero to 100 volts.

B. Phase Response

A block diagram of the phase measuring equipment is shown in Figure 36. A photograph of the test equipment setup is shown in Figure 37.

The phase measuring system consisted of a RANTEC Model ET-110U, wideband precision phase system driven from a General Radio Type 1209 BL variable frequency oscillator. The phase system was linear from 200 mc/s to 1000 mc/s to within ±3.0 degrees or 5 percent of meter reading difference whichever is greater. The advantageous feature of this instrument is that the signal generator can be swept in frequencies from 200 to 1000 mc/s and the resultant phase displayed on an oscilloscope. The reading is to within ±3 degrees of linear over that range using the reference line supplied with the unit.

The basic phase system, as shown in Figure 36, operates as follows. The power from the oscillator is split, part passing through a reference line and part through the unit under test. The phases at the output of these two signal paths are compared and the resultant phase difference indicated either on a meter or an oscilloscope. The output has a full-scale deflection of either 45 degrees or 5.8 degrees. Various attenuators are located in both paths to attenuate reflected signals. In order to sweep the General Radio Oscillator, a mechanical driver unit is required.

The object of the phase measurement is to determine the phase variation from linearity. This could be measured by two methods. First, if the reference line provided with the equipment is used, a plot of phase versus frequency will yield a line having a slope proportional to the delay through the unit under test.

To determine the variation from linear the slope must be subtracted out to plot this variation. A simpler and faster, but slightly less accurate, method is to provide a reference line whose electrical length is exactly the same as the unit under test. This assumes that the reference line is at least as linear as the desired unit linearity. Therefore, the phase variation from the two signal paths will be a measure of the unit's phase variation from linearity.

This latter technique was used to obtain the phase responses measured in this report. A high-quality coaxial cable of the approximate length was placed in the reference line. As the frequency was varied from 200 mc/s to about 350 mc/s, a line stretcher in the reference path was adjusted for minimum phase variation, i.e., maximum slope cancellation. The high-quality coaxial cable used in the reference

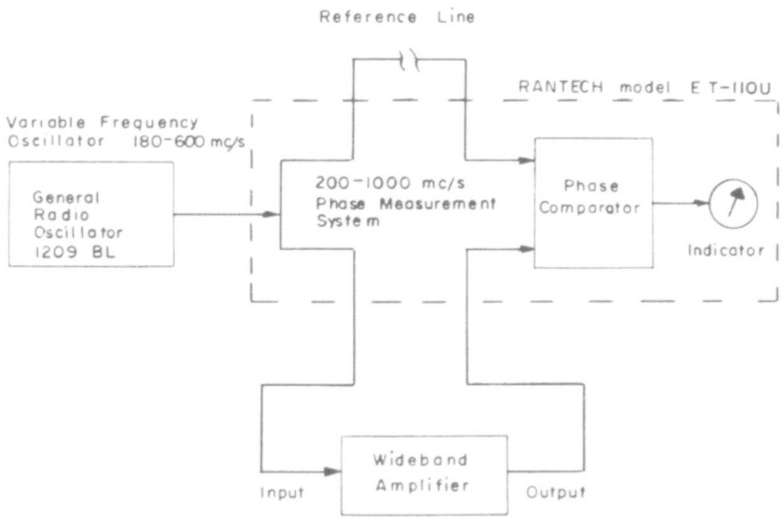


Figure 36. Phase Measurement Technique

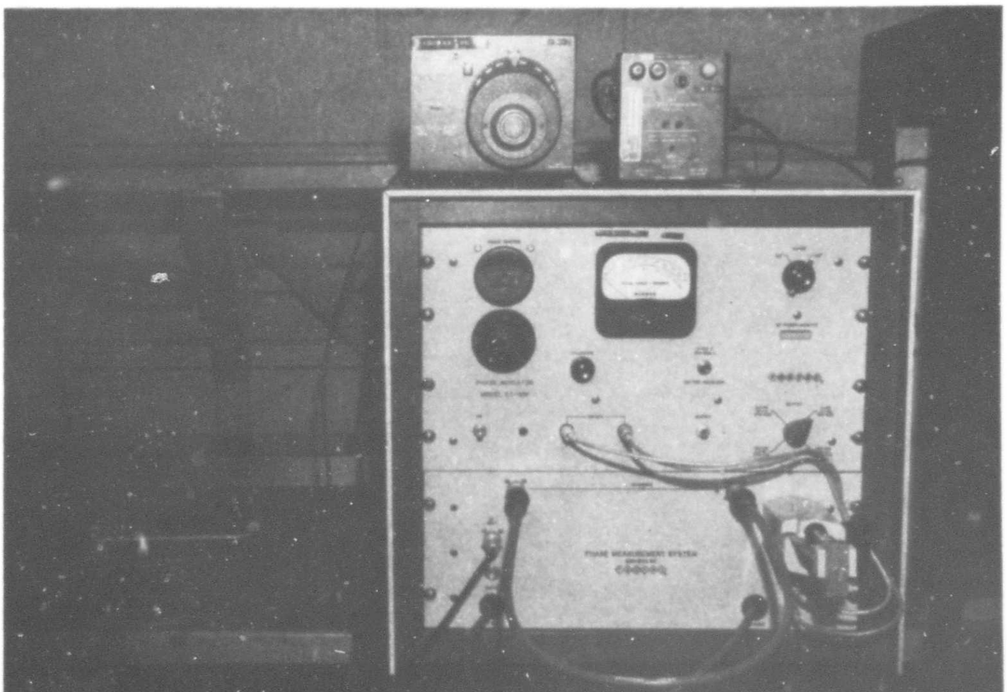


Figure 37. Photograph of Phase Measurement Equipment

line was General Radio Type 874-A2 which had a characteristic impedance of 50 ohms. This cable was obtained from the General Radio Transfer-Function and Emittance Bridge, Type 1607-A. The cable had General Radio connectors on each end and was designed to operate up to 1500 mc/s.

VI. PRACTICAL CONSIDERATIONS

There are a number of practical considerations that should be discussed. By far, the two most important are, in order of importance, the transistor, and the component layout.

A. Transistor Selection

A few of the more important parameters in transistor selection follow. When building wideband amplifiers, it is of utmost importance to select a transistor that will consistently yield the desired gain for a specified bandwidth. The critical transistor parameters are seen from the expression for the device's maximum power gain-bandwidth product f_{max}. This is the frequency at which the transistor's power gain is unity. Note that because the output impedance is higher than the input, power gain is possible even though the current gain is less than unity.

$$f_{max} = \sqrt{\frac{f_T}{8\pi \, r_{bb} \, C_{bc}}} \; .$$

f_T is the device's current gain-bandwidth product or that frequency where the current gain β is equal to unity. The term r_{bb} is the transistor's base resistance and C_{bc} is its base to collector-base capacitance. The product $r_{bb}C_{bc}$ ($r_b' \, C_c$ on data sheets) is the collector-base time constant. For a good high-frequency transistor, this time constant will vary between 1 to 60 psec.

The power gain-bandwidth expression above is based on the assumption that the driving source is matched to the input for maximum power transfer. The same is true of the output. For wideband use, this condition is almost impossible and should not be attempted as it is quite time-consuming and varies from device to device. This expression will yield values larger than are usable in practice and therefore must be reduced, although many manufacturers specify the parameters of this expression over a range of values; i.e., maximum, typical, and minimum. The typical value is strictly that and should be ignored. When selecting a transistor by f_T, the minimum or guaranteed value should be used. In general, most of the units will fall between the minimum and typical with few at the maximum value.

The same consideration is true of the collector-base time constant $r_{bb}C_{bc}$; its maximum value should be used to compute f_{max}. Some manufacturers specify a guaranteed f_t or f_{max} which should be used instead of the typical values. It is frustrating and time-consuming to strive for a given gain and bandwidth that is marginal for the transistor when a slightly better guaranteed device would yield the desired response with a minimum of effort. These considerations are particularly critical when the amplifier is to be mass-produced.

If a transistor's parameters are in doubt, they can easily be measured by use of a transfer-function and emittance bridge. The General Radio Type 1607-A is well suited for measuring the current gain β at various frequencies as well as Z_{in}, Z_{out}, r_{bb}, C_{bc}, etc.

B. Layout

Next in the line of importance is the layout of the components. It goes without saying that all leads should be short. Actually, this is somewhat misleading since it is the length of the signal path that is important. This distinction in terminology includes the signal path through the grounding medium; that is, the distance between grounding points must be short.

A typical example of this problem was encountered when an output BNC connector was mounted at right angles to the chassis in order to reduce the length of the center conductor connection to the circuit. Although this length was short (0.2 inch) the ground path was about three-quarters of an inch to the emitter bypass. The resultant amplifier response had a large resonant peak at the high frequency end. The output connector was remounted on the ground plane as close to the emitter bypass as possible, thereby reducing resonant peak.

The 2N918 transistors used have a fourth wire connected to the outside case. In the initial layout, the transistors were suspended above a ground plane by their leads. When the case was grounded to the ground plane by a #10 wire, the resonant peak was further reduced.

Such peaks are generally caused by the transistor's output capacitance resonating with various stray inductances. When higher frequency transistors are used, the frequency at which the peak occurs is increased. Often the loss associated with the inductance will increase with frequency sufficient to completely eliminate the peak. A recommended layout procedure would require:

- Mounting the transistors case in the chassis or ground plane;
- Locating the transistors physically close to each other; also mounting other components such as capacitors, connectors, etc. close to transistor cases;
- Using as small a physical size capacitor as possible; preferably, they should be good quality high-frequency capacitors.

Ceramic capacitors are generally resonant between 1 and 30 mc/s and should not be used for this reason.

C. Components

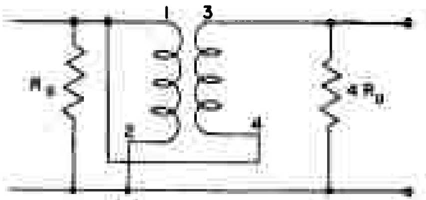
Wideband Impedance Transformer:

Often it is desirable to increase the output or input impedance of a transistor amplifier in order to increase its gain. For example, a grounded base amplifier has a unity current gain up to its alpha cutoff frequency. The use of a transformer to increase the load impedance seen by this collector will result in an increase in gain.

A conventional transformer cannot be used for wideband application because the interwinding capacity resonates with the leakage inductance to produce peaks in the response and thus limit its high-frequency response. Ruthroff [3] has described

a special broadband transformer that operates similar to a transmission line in which the coils are so arranged that the interwinding capacity is a component of the characteristic impedance of the line. The result is a small transformer with good high-frequency response.

The particular transformer of interest here is the 4:1 impedance transformer shown in Figure 38.



(a)

TRANSMISSION LINE FORM

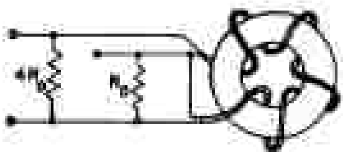

(b)

Figure 38. Wiring Diagram for 4:1 Impedance Transformer

The pair of wires which form the primary and secondary windings take the form of twisted pairs. The twisted pair is wound on a small ferrite toroid with windings closely spaced to maintain good coupling. In this configuration, the high-frequency response is determined by the length of the winding. The toroid forms used had an inside diameter of 0.08 inches, enabling small size and high-frequency operation. Ruthroff has shown that if the line length of the winding exceeds $\lambda/4$, the response will be down by more than 1 db and the response is zero at $\lambda/2$. The transformer is matched when $R_L = 4R_O$. It has been found by this author that the response can be made to either increase or decrease with frequency by manipulating R_L. Often, the presence of high-frequency peaks in an amplifier response using such a device is caused by improper transformer matching. This condition can be eliminated by shunting either the primary or secondary, depending on which is terminated by too large an impedance.

Ruthroff obtained responses from 0.2 to 715 mc/s (3 db). The low-frequency response depends on the permeability of the core and the number of turns. The larger the permeability, the fewer turns required to give a low-frequency response. For good high-frequency response, few turns are required. As few as one turn has been built by this author and found to perform nicely to 900 mc/s; however, the low-frequency response had to be sacrificed.

Capacitors:

As mentioned above, the use of disc ceramic bypass capacitors can produce sharp resonances between 1 and 30 mc/s and provide poor isolation at higher frequencies. A high-frequency capacitor that was found quite satisfactory and used in the experiments reported here was a 1000 pF discordant capacitor made by Allen-Bradley Co. Both feedthrough (Type FB2B) and standoff (Type SB4A) were used. These provide effective filtering to 1000 mc/s. A new type feedthrough, Type FW5N, made by Allen-Bradley is smaller and would be better than those used, however.

Fixed Resistors:

Allen-Bradley 1/4 watt, 5-percent carbon resistors were used throughout the experimental work and found to be satisfactory to 900 mc/s. No tests were performed above this frequency. Half-watt carbon resistors were tried at several points in the high-frequency circuitry and no noticeable effects were noted. However, their size makes them bulky to handle. The 1/4 watt resistors are about the right size for high-frequency work.

Adjustable Resistors:

Small adjustable noninductive resistors would be highly desirable in such locations as the feedback path of the collector-base feedback amplifier. Extreme care must be used with such components since they are inherently inductive. In addition, their bulky size increases the chances of stray capacitive interaction which can produce bothersome peaks within the passband. About the only place that such a component should ever be used is in the feedback path of the collector-base feedback amplifier where a series inductance is usually added. Even here, extreme care must be observed.

Inductors:

At the frequencies we are considering here, the inductors should be air wound with a small diameter (a half-watt resistor was used as a form to yield a satisfactory diameter). The use of slugs to vary inductance is not considered advisable. The presence of slugs not only produces loss within the coil but the added stray capacitance could create resonant peaks. About the only way to vary the inductance is to either cut off turns or short adjacent turns with solder. The coupling between turns is quite low and the shorting of turns appeared to be satisfactory.

Connectors:

BNC connectors were used throughout this work and did not appear to produce severe reflections.

Coaxial Cable:

RG-58A and C coaxial cable was used between generator, amplifier, and detector. This cable has a nominal characteristic impedance of 51.0 ohms and a capacitance of 29 pF/ft. Care must be taken not to place a soldering iron on the cable. A burned spot can result in excessive reflections and peaks and nulls across the band.

VII. CONCLUSIONS AND RECOMMENDATIONS

This investigation proves the feasibility of a wideband, electronically-controlled, digital delay line for application in steering wideband array antenna systems. The approach taken was to use wideband transistor amplifiers as switches to direct the wideband signal either through or around the delay line. It is the bandwidth of these amplifiers that determines the system bandwidth. By using wideband amplifiers in place of diode switches: (1) each delay line can be terminated better into its characteristic impedance over the frequency band of interest; (2) each delay line increment is isolated from the next; (3) with the inclusion of amplifiers, the total input-output gain can be made greater than unity.

The digital delay line described in this report is designed to operate at the i-f frequency of the array antenna. It is also proved that wideband i-f time delay steering of array antennas is feasible.

The frequency band covered by this variable delay unit is from 50 mc/s to 450 mc/s yielding an instantaneous bandwidth of 400 mc/s. The gain variation from 50 mc/s to 400 mc/s and between bits in the worst case is down one db with a maximum phase error of two degrees. At a frequency of 450 mc/s, the amplitude variation is 2 db and the phase error has increased to 10 degrees in the worst delay setting.

Coaxial cable (RG-58A and C) was used as the basic delay element. Two different cable lengths were used in the unit test. In the first section, a cable length of about 16 ft. was used and in the second section a 6-ft. length was used. With these cables to determine incremental delays, the delay variations obtainable included 0, 12.61, 28.92 and 41.53 nanoseconds.

The time required to switch between bits was found to be 50 nanoseconds. Although this is far better than required in an actual system, the limiting element appeared to be the transistor switch itself.

Since the primary objective was to prove feasibility, no attempt was made to maximize the bandwidth. By using better quality high-frequency transistors, the bandwidth could be extended substantially. With the state of the art in high-frequency transistors increasing each year, it should be feasible in the next few years to extend the bandwidth into C-band at a reasonable cost; i.e., 15 to 20 dollars per transistor.

The major problem areas, however, are not in the bandwidth of the amplifiers but in obtaining a near-perfect delay line termination across the band. If the delay line is not properly terminated, ripples in the amplitude response are present. A VSWR of 1.1 will produce a 1 db ripple across the pass band. When several delay bits are used, these ripples add and subtract at different points in the band to produce ripples as high as 3 db for two bits. This problem is discussed in detail. Therefore, future work should be directed at how to properly terminate a delay line into a transistor amplifier in order to reduce the VSWR. The method used here to reduce this ripple was to place an attenuator in each delay line. This attenuated the reflected wave sufficiently to reduce the ripple below the desired level. This is the brute force approach, however. The use of wideband isolators or circulators, although expensive, would be desirable. Another approach not investigated here but which bears investigation is the use of strip lines where the impedance of the line can be changed to match the load. As the bandwidth is increased, the layout problem will become more critical. The use of strip line construction would be a necessity and should be investigated further. Other approaches also bear investigation.

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13 ABSTRACT

This report presents the detailed technical analysis, experimental results, and problems encountered in the design and construction of a four-bit digital delay line having an instantaneous, nondispersive, and lossless bandwidth of 400 mc/s. The frequency range covered was from 50 to 450 mc/s. The signal was switched either through or around the different time delay elements. The switches consisted of wideband amplifiers which minimize amplitude and phase fluctuations across the band and between the different signal paths. Switching was performed by purely electronic means with switching time less than 50 nanoseconds. Amplitude variations up to 400 mc/s were less than 1 db with a phase error of 2 degrees. At 450 mc/s the errors were 3 db and 10 degrees, respectively.

Also covered is the use of such a device for i-f time delay steering of wideband array antennas. Problems encountered in properly terminating wideband delay lines and component selection and layout are discussed.

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14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Transistor Amplifiers						
Wideband Amplifiers						
Single Stage						
Cascaded Stages						

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